Five-Level Unidirectional T-Rectifier for High Speed Gen-Set Applications

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***Abstract*—Multi-level power electronic topologies are being proposed in the recent technical literature for use in power generating units. Especially when the reduction of the power filter overall dimensions and the lowering of current and voltage waveform ripple and total harmonic distortion are considered of primary importance. This is the case of high speed gen-set units, where recent design techniques on high rotational speed permanent magnet synchronous generators have significantly reduced the inductance even for industrial voltage rated applications. The paper deals with a five-level unidirectional T-rectifier; the proposed topology is theoretically investigated, simulation results and losses analysis are achieved with reference to an IGBT phase leg module which has been manufactured on purpose and tested.**

***Index Terms* – AC-DC power converters, harmonic distortion, power losses, high frequency.**

I. INTRODUCTION

The scenario of electric power generating systems is rapidly moving toward using of high rotational speed machines because of the growing interest in the more electric aircraft (MEA) as well in the distributed electric generation (DEG) and automotive applications. To this purpose, electric drives having high rated speed are being proposed in the recent technical literature for use in combination with micro-gas and air turbines to arrange power generating units having rated power in the range from few kilowatts to hundreds kilowatts [1]-[2]. Main equipment in such emerging generating units are the electrical generator, the AC-DC power electronic converter, and the output inverter in case of ac output load both for grid connected and for stand-alone power grid. As well, the control algorithm of the generating unit plays a key role for regulating electrical voltages and currents, which have high frequency fundamental order up to 1-2 kHz. The paper investigates the 3-phase 5-level unidirectional T-rectifier topology (5L T-RECT) to be used in pair with a high rotational speed permanent magnet synchronous generator (PMSG).

Three-phase supplied AC-DC power converters are widely used in many applications, such as variable speed drives, UPS, data centers and telecom power supplies [3]. The rectifier main design objectives are efficiency, size, reliability and cost. Recently, the growing attention in MEA and DEG boosted the interest in electric drives having high rotational speed and in the related power losses investigation; as a result, the rectifier input current harmonics content has become a more and more important design criterion [4]. In variable speed applications, the DC-bus voltage has often to be constant and greater than the input voltage. Numerous different rectifier topologies have been presented in literature and used for many applications. Advanced three-level rectifier as Vienna, Swiss and T-type topologies, as well hybrid rectifier configurations based on such topologies, have been investigated mainly for grid connected 3-phase PFC systems; recently, the achieved analyses have also been successfully extended to aircraft applications [5]-[6].

A 5-level boost rectifier topology is presented in this paper with reference to high-speed gen-set applications. A unidirectional T-rectifier based configuration is chosen for the reduced switch count, as well an additional DC-bus voltage balancing circuit is considered in order to assure balancing of DC-link capacitors voltages, regardless on variation of the rectifier load and both the generator and the DC-bus voltage. The investigated configuration exhibits same number of switches as a conventional 3-level T-type inverter, when the additional DC-bus voltage balancing circuit is not considered. Higher number of levels fits the requirements imposed by the high fundamental frequency applications. As stated in Section III, the switching devices of the proposed 5-level topology are rated for either ¼ or ½ of the output dc link voltage.

II. HIGH SPEED GEN-SET APPLICATIONS

High-speed gen-set units play an important role in the field of power generating units, also on board of vehicles and aircrafts, because of their reduced volume and weight as well high efficiency in particular in case of direct drive configurations. In MEA applications, high-speed electrical generators are directly coupled to aircraft turbines in order to provide, through the controlled 3-phase rectifier, power supply to 540V DC-bus as schematically depicted in Fig. 1a. In case of the automotive applications, the increased electrical power demand inevitably results in increased fuel consumption. However, from recognizing that the ICE exhaust gases still retain a significant amount of energy being usually wasted, substantial fuel saving can be achieved by

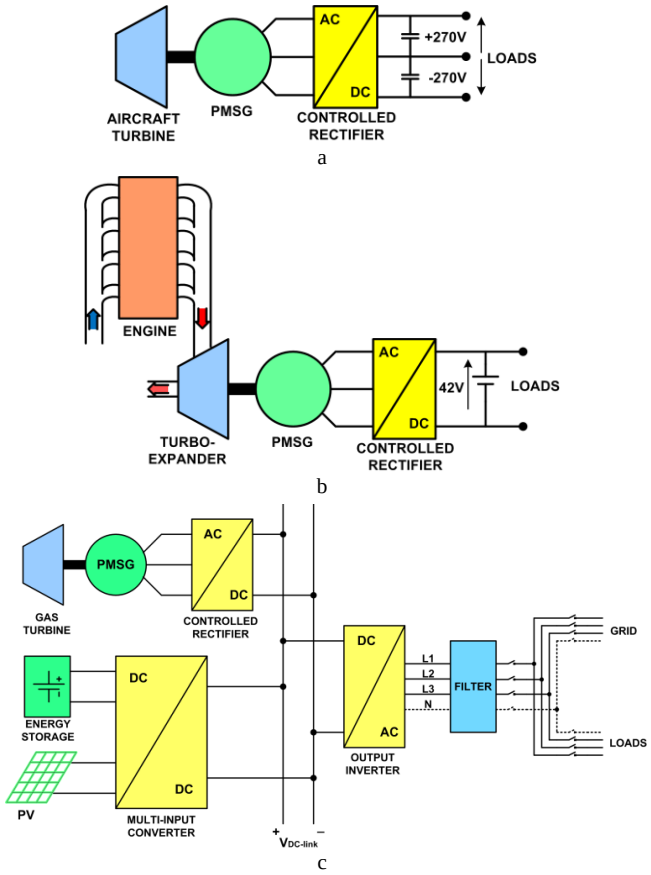

Figure 1. Schematic layout of high speed gen-set for emerging applications; a) aircraft, b) automotive, c) distributed energy generation.

using of a radial turbo-expander, which can provide recovery of the kinetic energy available from the ICE exhaust gases to directly drive an electrical generator as it is depicted in Fig. 1b. The high-speed electrical generator output is rectified through a controlled rectifier in order to suitably supply the power-net architecture within the variable rotating speed region of the radial turbo-expander. Also in DEG systems high-speed gen-sets, which are driven by gas turbines, are often proposed to integrate renewable energy generating units and possible storage units as it is shown in Fig. 1c.

Recent advancements in magnetic materials and motor design techniques have made the PMSG an excellent candidate for high speed generating units. In PMSG, the main flux is produced by the magnets either mounted on the surface of or buried inside the rotor. Because the magnets do not carry current, copper loss is eliminated from the rotor. Further, PMSG can operate at nearly unity power factor. Hence, permanent magnet machines have higher efficiency compared to induction machines. Moreover, it is easy to achieve high-performance torque control with PMSG.

However, due to a long effective air gap, PMSGs tend to have low inductance. In high rotational speed applications, because of the relevant frequency value for the first harmonic order, the air gap is intentionally made quite large to reduce the flux harmonics caused by stator slots and thus the resultant iron loss in the stator can be significantly decreased. Recent design techniques on high rotational speed PMSG, such as the use of ironless stator structure, have reduced the inductance even further below 100 µH for industrial voltage rated applications. These types of very low inductance PMSG can provide fast current control response, which is favorable for most applications. As well, for any operating condition set by the alternator input torque and speed and for a given voltage of the DC-bus, the lower is the alternator synchronous inductance, the lower will be the RMS value of the fundamental frequency current that circulate in the power switches and diodes of the controlled rectifier [1].

On the other hand, the low inductance imposes a stringent current regulation demand for the AC-DC power electronic converter to produce a phase current with an acceptable level of current ripple, which is typically required to be lower than 20% of the RMS current value for many applications.

In high-speed gen-set, for low power (up to a few kW) applications, MOSFETs are usually employed because they can effectively switch at up to hundreds of kHz, which can handle moderately low inductance (a few tens µH) electrical machines. As the power level reaches several tens of kW the preferred switching device is the IGBT, which is typically available in two or six-pack modules. IGBT modules can only switch at up to 20 kHz, which is not sufficiently high for low inductance PMSGs when conventional 2-level power electronic converters are considered. Multilevel topologies therefore seem to be a good option in power generating units with high frequency value of the voltage first harmonic order.

The 5-level unidirectional T-rectifier, which is first theoretically investigated in the paper, is proposed for the applications of Fig. 1. Simulation and experimental results are described in the following; whereas, the losses analysis is achieved thanks to the IGBT phase-leg module manufactured on purpose by Semikron®.

III. Five-Level Boost Rectifier

Circuit diagram of the proposed five-level unidirectional T-rectifier is depicted in Fig. 2. The rectifier consists of 5 functional blocks: 1) input filter inductors L_{0A}, L_{0B} and L_{0C}, 2) three-phase diode bridge, 3) a set of bidirectional switches connected between the diode bridge and the DC-bus capacitors, 4) a set of four series connected DC-bus capacitors C_{B1}...C_{B4}, and 5) two voltage-balancing devices. The rectifier load is connected across plus and minus DC-bus rail. Operating principle of the rectifier is briefly described in the following sub-section.

A. *Theoretical background of the topology*

1) *Voltage and current definition*

The generator is a symmetrical three phase PM generator, having the phase-to-neutral voltages and the DC-bus voltage as follows

$$v_{(A,B,C)}(t) = \sqrt{2}U_{IN}\sin\left(\omega_m t - (p-1)\frac{2\pi}{3}\right) \text{ and}$$
$$V_{BUS} = k_{BOOST}\,2\sqrt{2}V_{IN} \quad (1)$$

where $p=1,2,3$ is the phase order, k_{BOOST} is the rectifier boost coefficient and V_{IN} is the rms value of the input phase voltage. Moreover, taking in consideration the basic modes of operation of the investigated converter topology and being I_{IN} the rectifier rms current, the fundamental components of the input phase currents can be written as

$$i_{(A,B,C)}(t) = \sqrt{2} I_{IN} \sin\left(\omega_m t - (p-1)\frac{2\pi}{3}\right). \quad (2)$$

Whereas, with reference to the PWM modulation techniques for multilevel inverters [6, 7], the rectifier modulation index can be defined in following general form

$$m_{(A,B,C)}(t) = m_0 + \frac{1}{2}\left(1 + M \sin\left(\omega_m t - (p-1)\frac{2\pi}{3}\right)\right), \quad (3)$$

where M is the modulation depth and m_0 is offset of the modulation index.

2) Operating sectors

For the sake of simplicity, the rectifier is modeled by one-phase equivalent circuit diagram as it is depicted in Fig. 3. The DC-bus capacitors are modeled by constant voltage sources v_{CB1}, v_{CB2}, v_{CB3}, v_{CB4}, where the DC-bus partial voltages are assumed to be equal.

$$v_{CB1} = v_{CB2} = v_{CB3} = v_{CB4} = \frac{V_{BUS}}{4}. \quad (4)$$

Fig. 4 shows the rectifier input phase-to neutral voltage v_A and the rectifier switched voltage v_{A0}. Notice the four DC-bus voltage levels and the four sectors that correspond to the ratio of the input voltage and DC-bus voltage.

Sector 1 - If the input phase-to-neutral voltage is negative and falls in the range

$$-\frac{V_{BUS}}{2} \le v_A < -\frac{V_{BUS}}{4}, \quad (5)$$

the rectifier operates in the sector 1. The input current i_A is negative and it commutes between diode D_{AA} and bottom inner switch S_{A1}, Fig. 5a. The rectifier bridge input voltage v_{A0} takes two discrete values *0* and $¼V_{BUS}$.

Sector 2 - If the input phase-to-neutral voltage is negative and falls in the range

$$-\frac{V_{BUS}}{4} \le v_A \le 0, \quad (6)$$

the rectifier operates in the sector 2. The input current i_A is negative and it commutes between the bottom-inner switch S_{A1} and the inner switch S_{A2}, Fig. 5b. The rectifier bridge input voltage v_{A0} takes two discrete values $¼V_{BUS}$ and $½V_{BUS}$.

Sector 3 - If the input phase-to-neutral voltage is positive and falls in the range

$$0 < v_A \le \frac{V_{BUS}}{4} \quad (7)$$

the rectifier operates in the sector 3. The input current i_A is positive and it commutes between the inner switch S_{A2} and the top-inner switch S_{A3}, Fig. 5c. The rectifier bridge input voltage v_{A0} takes two discrete values $½V_{BUS}$ and $¾V_{BUS}$.

Sector 4 - If the input phase-to-neutral voltage is positive and falls in the range

$$\frac{V_{BUS}}{4} < v_A \le \frac{V_{BUS}}{2} \quad (8)$$

the rectifier operates in the sector 4. The input current i_A is positive and it commutes between the top-inner switch S_{A3} and the top diode D_{AB}, Fig. 5d. The rectifier bridge input voltage v_{A0} takes two discrete values $3/4V_{BUS}$ and V_{BUS}.

3) Generator current ripple versus number of levels

The generator current ripple of a N-level rectifier is inversely proportional to the input filter inductance and number of levels N

$$\Delta i_A = \frac{k}{L_A (N-1)}, \quad (9)$$

where L_A is total input inductance and k is a coefficient that depends on the switching frequency, DC-bus voltage and modulation strategy. In order to reduce the current ripple and stress on the generator, an additional inductor should be used or number of levels increased. Implementation of an additional filter inductor is not an option because of additional cost, losses and weight. The only option is to increase of number of levels, whereas the state of the art solutions are 2-level and 3-level Neutral Point Clamped (NPC) topologies [1]. According to the analysis conducted in sub-section above, the proposed rectifier bridge (phase-to-minus DC-bus) voltage is

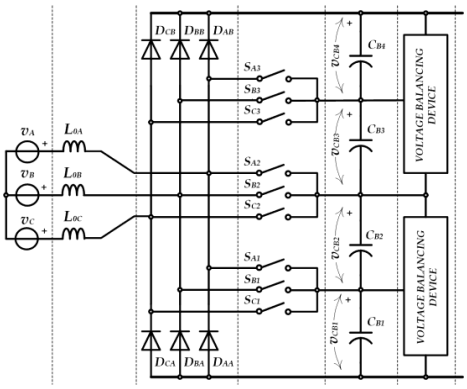

Figure 2. 5L T-RECT with the external balancing circuit.

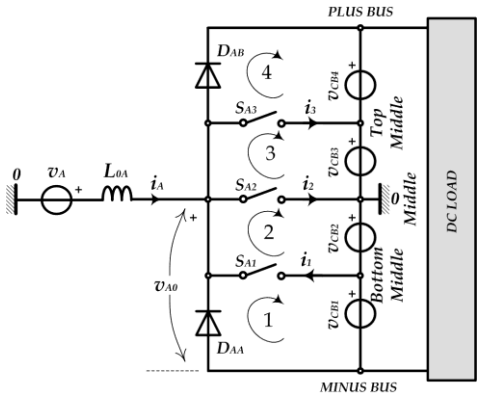

Figure 3. Simplified equivalent circuit of one phase of the 5L T-RECT.

a 5-level voltage. The voltage levels are: 0, ¼V_{BUS}, ½V_{BUS} ¾V_{BUS} and V_{BUS}.

Fig. 6a shows the comparison of the generator current ripple versus modulation index for a 3-level and a 5-level rectifier. As predicted by (9), 5-level rectifier has 50% of current ripple compared to 3-level rectifier. However, the current ripple itself is not of great interest. The generator losses caused by the current ripple are of the higher interest. Fig. 6b shows the comparison of the generator current ripple losses versus modulation index for a 3-level and a 5-level rectifier. The 5-level rectifier has significantly lower current ripple losses when compared to 3-level rectifier (25% versus 100%). This brief comparison clearly shows the benefit of the 5-level versus the 3-level topology.

B. Inner switches realization

The top-side inner switch S_{A3} is voltage bidirectional and current unidirectional switch. The current direction is from the diode rectifier to the DC-bus capacitors. Thus, the switch can be arranged as a series connected MOSFET or IGBT M_{x32} and diode D_{x31}, as depicted in Fig. 7a. The switch voltage rating is ¼V_{BUS}, while the diode voltage rating is ¾V_{BUS}.

The inner switch S_{A2} is voltage and current bidirectional switch. A possible arrangement using two MOSFETs or IGBTs is depicted in Fig. 7b. The switches voltage rating is ½V_{BUS}.

The bottom-side inner switch S_{A1} is voltage bidirectional and current unidirectional switch. The current direction is from the DC-bus capacitors to the diode rectifier. The switch can be arranged as series connected MOSFET or IGBT M_{x11} and diode D_{x12}, as depicted in Fig. 7c. The switch voltage rating is ¼V_{BUS}, while the diode voltage rating is ¾V_{BUS}.

Each switch is commutated through a specific gate driver. In particular, inner switch S_{A2} requires two separate gate drivers in order to assure all the intermediate voltage levels even when phase displacement between the rectifier input line current and phase voltage can occurs.

C. Capacitors voltage balancing issue

1) Problem definition

Mid-point voltage balancing is a well-known issue in application of 3-level NPC converters [8]. The converter injects a current in the capacitors mid-point. Due to no-idealities in the switching, the injected average current may cause deviation of the voltage distribution among series connected capacitors. A well-established solution is the active control of the mid-point voltage via the modulation index offset m_0 as the control variable. The 5-level rectifier presented in this paper has slightly different structure from the state of the art 3-level NPC. Equivalent circuit diagram of the DC-bus is depicted in Fig. 8, where BLC stands for general purpose voltage balancing circuit. Please notice three nodes; 1) bottom mid-point, 2) mid-point and 3) top mid-point. The rectifier injects currents i_1, i_2 and i_3 into the DC-bus. To provide normal operation of the rectifier, the capacitors voltages must be balanced regardless on variation of the rectifier load and both the generator and the DC-bus voltage.

2) Mid-point voltage

It can be proven that average value of the mid-point current i_2 is a function of the modulation index offset m_0,

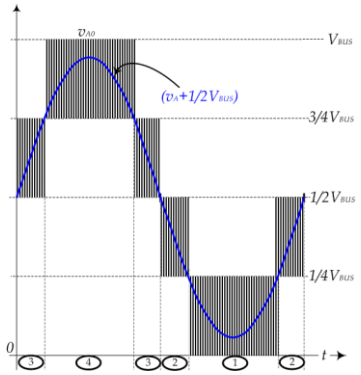

Figure 4. The phase-to-neutral voltage v_A and the bridge voltage v_{A0}.

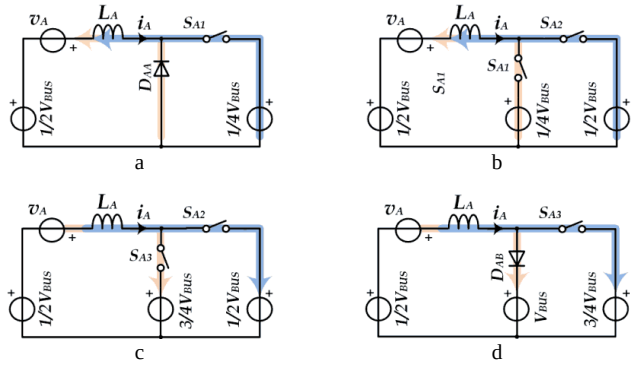

Figure 5. Operating sectors. a) Sector 1; b) Sector 2; c) Sector 3; d) Sector 4.

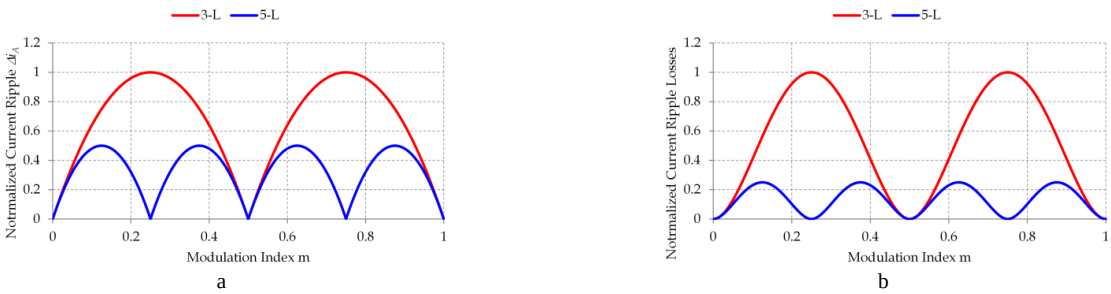

Figure 6. a) Current ripple Δi_A; b) normalized current ripple losses versus modulation index m.

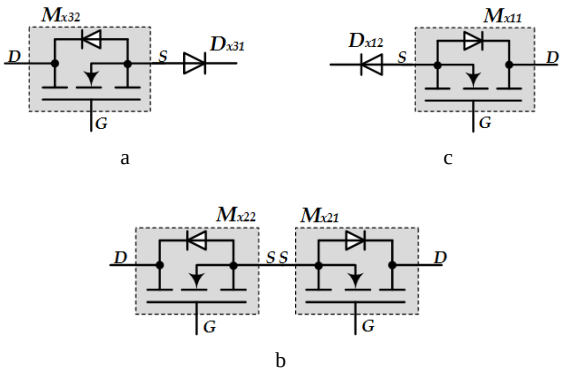

Figure 7. Realization of the inner switches S_{A1}, S_{A2} and S_{A3}

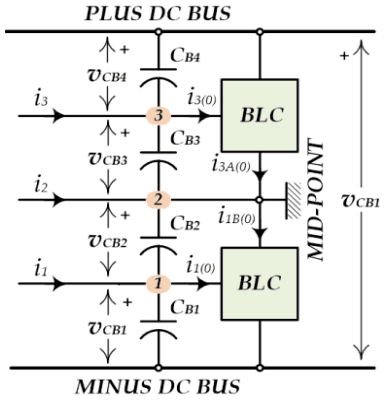

Figure 8. Equivalent circuit of the DC-bus including voltage balancing circuit.

$$\langle i_2 \rangle = \frac{1}{T}\int_0^T i_2 dt = m_0 K_0 , \qquad (10)$$

where T is fundamental period and K_0 is a coefficient that depends on the rectifier input current. Since the mid-point average current $\langle i_2 \rangle$ is a function of the modulation index offset m_0, it is obvious that the mid-point voltage is controllable by introducing a zero sequence in the modulating signal according to multilevel NPC modulation techniques [9, 10]. Hence, controlling the mid-point current $\langle i_2 \rangle$, it can be achieved that

$$v_{CB1} + v_{CB2} = v_{CB3} + v_{CB4} . \qquad (11)$$

3) Partial (bottom and top) mid-point voltages

Partial mid-point voltages are voltages across individual DC-bus capacitors. The mid-point voltage condition (11) is not a guaranty that the voltages across the DC-bus capacitors are equal. It can be proven that average value of the bottom mid-point current i_1 (12) is negative, while the top mid-point average current i_3 is positive

$$\langle i_1 \rangle = \frac{1}{T}\int_0^T i_1 dt < 0 , \langle i_3 \rangle = \frac{1}{T}\int_0^T i_3 dt > 0 \qquad (12)$$

where T is the fundamental period of the generator sinusoidal voltage. The top and bottom mid-point currents are not controllable variables. Simple speaking, the capacitor voltages cannot be controlled by the modulation index offset m_0. The currents $\langle i_1 \rangle$ and $\langle i_3 \rangle$ must be re-injected (canceled) by an additional voltage balancing circuit. Details of such a balancing circuit are given in following section.

IV. DC-Bus Voltage Balancing Circuit

As already mentioned in section III.C, the role of the balancing converter is to balance the voltages v_{CB1}, v_{CB2}, v_{CB3}, and v_{CB4}. Circuit diagram of the balancing converter is given in Fig. 9a. For the sake of simplicity, let's consider only the bottom side balancing converter. As discussed in [11], the balancing converter is nothing more than a variant of a switched capacitor converter. A switch leg S_{2A} S_{2B} is connected across the capacitor C_{B2}, and a diode leg D_{1A} D_{1B} is connected across the capacitor C_{B1}. The capacitor C_{S12} is the main switched capacitor that transfers the energy from C_{B2} to C_{B1}. The inductor L_{S12} is an auxiliary inductor used to reduce conduction losses and achieve Zero Current Switching (ZCS) condition [12]. The switches S_{2A} S_{2B} are driven with complementary control signals at period T_{S2}. The duty cycle d is constant, around 50%.

A. Analysis

For simplicity of the analysis, one can assume that the capacitors C_{B1} and C_{B2} are large enough to maintain the voltages v_{CB1} and v_{CB2} constant over one switching cycle T_{S2}. Also, the switches and the diodes are modeled by constant voltage sources V_S and V_{DF}. One complete cycle T_{S2} can be divided into four stages, namely stage A to stage D.

Stage A - The switch S_{2B} is closed at the instant $t=0$. The capacitor C_{S12} is charged from v_{CB2} via the switch S_{2B}, diode D_{1B} and the inductor L_{S12}. The current i_{R12} increases toward the peak I_{R12}. Once the current reaches the maximum, the current starts decreasing towards zero following the resonance of the $L_S C_S$ circuit.

Stage B - The current i_{R12} reaches zero and diode D_{1B} is blocked at the moment $t=T_0/2$. The current remains zero until commutation of the switch S_{2A} is accomplished.

Stage C - The switch S_{2A} is closed at the moment $t=T_{S2}/2$. The capacitor C_{S12} is discharged into v_{CB1} via the switch S_{2A}, diode D_{1A} and the inductor L_{S12}. The current i_{R12} increases in negative direction with respect to the direction in Fig. 9b. After reaching the maximum, the current starts decreasing towards zero following the resonance of the $L_S C_S$ circuit.

Stage D - The current i_{R12} reaches zero and diode D_{1A} is blocked at the moment $t=T_{S2}/2+T_0/2$. The current remains zero until the commutation of the switch S_{2B} is accomplished at the moment $t=T_{S2}$. At this point, one switching cycle is completed.

B. Voltage balancing capability

Let's consider the top side balancing converter. The balancing converter can be considered as a series resonant converter that operates in discontinuous conduction mode (DCM), type 1 [11].The input is voltage v_{CB3} while the output is voltage v_{CB4}. The voltage gain of series resonant converters operating in DCM type 1 is unity, regardless on the load and the switching frequency.

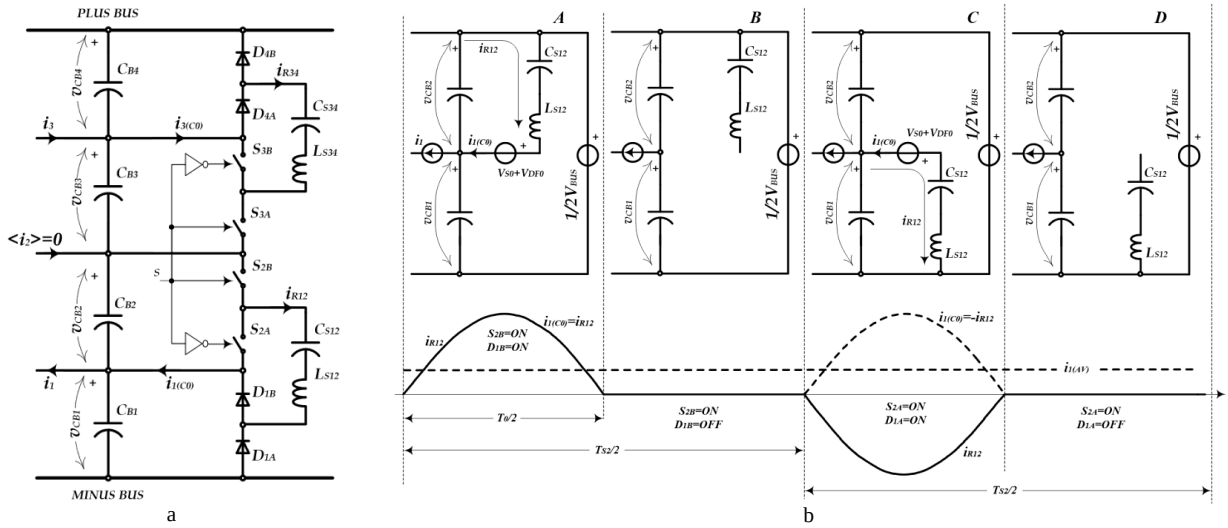

Figure 9. a) Circuit diagram of the balancing converter based on ZCS switched capacitor converter. b) Different topological stages of the converter. A) S_{2B}, D_{1B} are conducting, B) S_{2B} is conducting D_{1B} is blocking, C) S_{2A} and D_{1A} are conducting, and D) S_{2A} is conducting D_{1A} is blocking.

$$M = \frac{v_{CB4}}{v_{CB3} - (V_S + V_{DF})} = 1, \tag{13}$$

where V_S and V_{DF} are respectively the switch and the diode voltage drop.

It can be assumed that the mid-point voltage is well controlled by the rectifier inner control loop via the modulation index offset m_0. Hence, from (11) and (13) and under the assumption of (4), it can be found that the capacitor voltages are

$$\begin{aligned} v_{CB1} = v_{CB3} &= \frac{V_{BUS} + 2(V_S + V_{DF})}{4}, \\ v_{CB2} = v_{CB4} &= \frac{V_{BUS} - 2(V_S + V_{DF})}{4} \end{aligned} \quad . \tag{14}$$

As it can be seen from (14), the bottom to the top capacitor voltage ratio is constant regardless to the current i_1. Hence, the voltages are self-balanced and there is no need for direct measurement and control of the voltage distribution.

V. Power Converter Losses Analysis

In order to validate the technical solutions adopted for the proposed 5L T-RECT, simulations have been achieved with reference to the electric drive operating specifications of Table I. The model takes into account the actual characteristics of all the devices as they can be obtained from the data sheets. The investigation is carried out with reference to the circuit diagram of Fig. 10, where each phase leg is accomplished through a Semitop4 package module purposely manufactured by Semikron®. Each phase leg makes use of four high-speed IGBTs rated 50A-650V (die Infineon IGC16T65U8Q), four freewheeling Si rapid switching diodes rated 60A-650V (die Infineon IDC08D65Q8), and four SiC Schottky diodes rated 60A-1200V (die Infineon IDC08S120). The resonant balancing circuit is instead achieved through the series connection of SK75GB066T modules, rated 60A-600V, and

TABLE I. Operating Specifications for PMSG and 5L T-RECT

Rated mechanical input power [W]	17000
Rated speed [rev/min]	15000
Rated phase EMF [Vrms] @ rated speed	270
Rated phase current [Arms] @ rated torque	21
Fundamental frequency [Hz]	750
Switching frequency [kHz]	12
Voltage balancing circuit switching frequency [kHz]	20

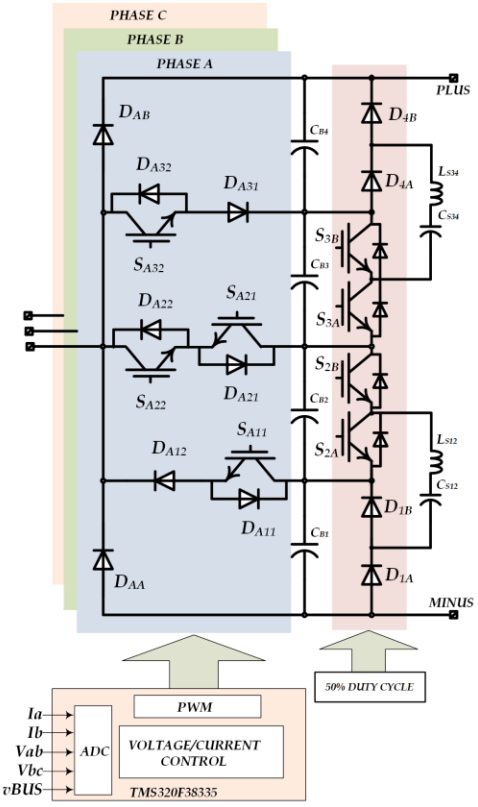

Figure 10. Circuit diagram of the 5L T-RECT prototype

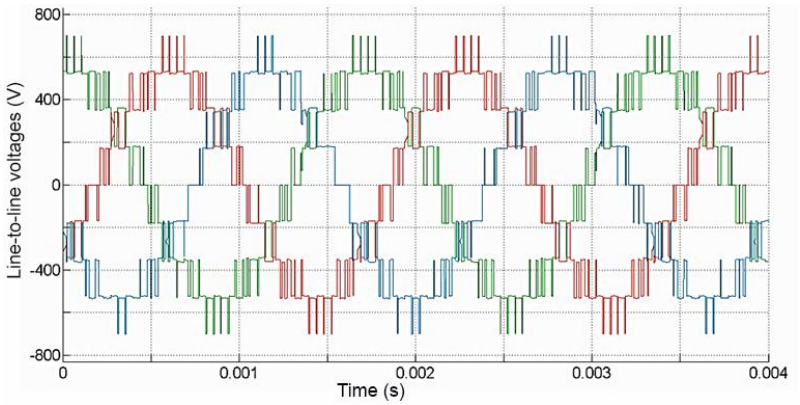

Figure 11. 5L T-RECT line-to-line voltages.

4μH and 16μF as resonant total inductance and total capacitance respectively. Fig. 11 shows the 5L T-RECT line-to-line voltage at high modulation index to fully highlight the available five levels.

With reference to the nomenclature as it is shown in Fig. 10, achieved devices losses are displayed in the following figures as a function of the modulation index and keeping constant at its rated value the rectifier input phase current. This means that the electrical generator is supposed to supply power at constant torque and variable rotating speed. Considering the circuit symmetry, the components of the same pair exhibit the same losses: D_{AA}/D_{AB}, D_{A12}/D_{A31}, S_{A11}/S_{A32}, S_{A21}/S_{A22} and D_{A21}/D_{A22}. Same consideration can be done for the DC-link capacitors, where the pairs are top/bottom and top-middle/bottom-middle.

The efficiency of the proposed configuration is evaluated considering four different junction temperatures for the devices with reference to the data-sheet provided by the components manufacturer. Efficiency results are shown in Fig. 12 for six values of the converter modulation index (m_A). Losses are achieved at 12 kHz switching frequency, phase peak current is set at 30A, whereas almost unity power factor and phase disposition PWM modulation with triangular third harmonic injection are considered.

According to the selected DC-link capacitors, estimated power losses have been plotted in Fig. 13a with respect to the converter modulation index. Losses distribution between top and top-middle capacitors is highly dependent on the operating conditions. In fact, when m_A is below 0.5, power is transferred using the middle leg and the top-middle capacitors. On the contrary, when m_A is above 0.5, top-leg is starting transferring power to the DC-link and then losses in the top capacitors increase. Switching devices and diodes losses distribution is shown in Fig. 13b to Fig. 13f, where constant junction temperature of 100°C is considered for all the devices.

Fig. 13b depicts both conduction and switching losses related to the S_{A22} IGBT. Being part of the middle-leg, the conduction losses reduce when the modulation index raises, because the average switch on-time decreases at increasing modulation index values (i.e. increasing electrical generator both rotational speed and phase EMF) and lower boost effect is required. Switching losses are kept constant for m_A lower than 0.5, being the phase peak current constant and because the middle leg commutates during the entire fundamental period. When m_A exceeds 0.5, the middle leg starts to not switch during the peak of the phase voltage waveform; further, phase current flow moves from middle leg to both top and bottom legs. As a consequence, strongly reduction of both conduction and switching losses is experienced in the middle leg for high modulation indexes. Power losses related to the diode D_{A21} in series with S_{A22} are shown in Fig. 13c. Recovery losses are negligible as diode D_{A21} (as well diode D_{A22}) turns off at either zero current or zero voltage. As a result, less expensive Si diodes instead of SiC ones have been selected as freewheeling diodes for the middle leg. Concerning losses dependence on the modulation index, it closely resembles the previously described behavior related to middle leg switches.

Concerning the T-outer legs, for $0<m_A<0.5$, the IGBTs S_{A11} and S_{A32} result in no switching losses as depicted in Fig. 13d. As soon as m_A exceeds 0.5, IGBTs starts commutating with constant switching losses because investigation is carried out with constant phase peak current. Conduction losses of IGBTs in T-outer legs show an increasing trend for $0<m_A<0.5$ and then a decreasing trend for m_A greater than 0.5, when input rectifier diodes D_{AA} and D_{AB} start conducting. T-outer legs diodes D_{A12} and D_{A31} are based on SiC devices and exhibit only conduction losses. According to the described

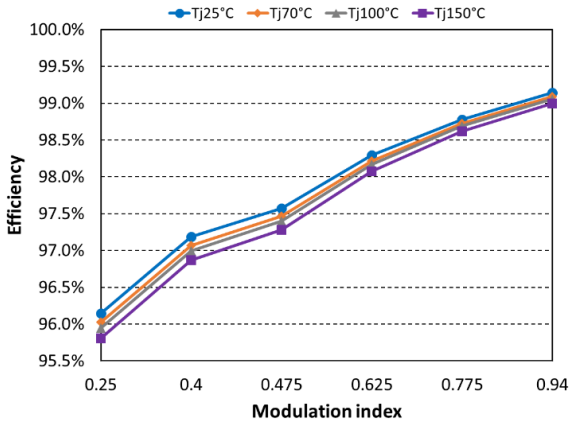

Figure 12. 5L T-RECT efficiency vs. converter modulation index.

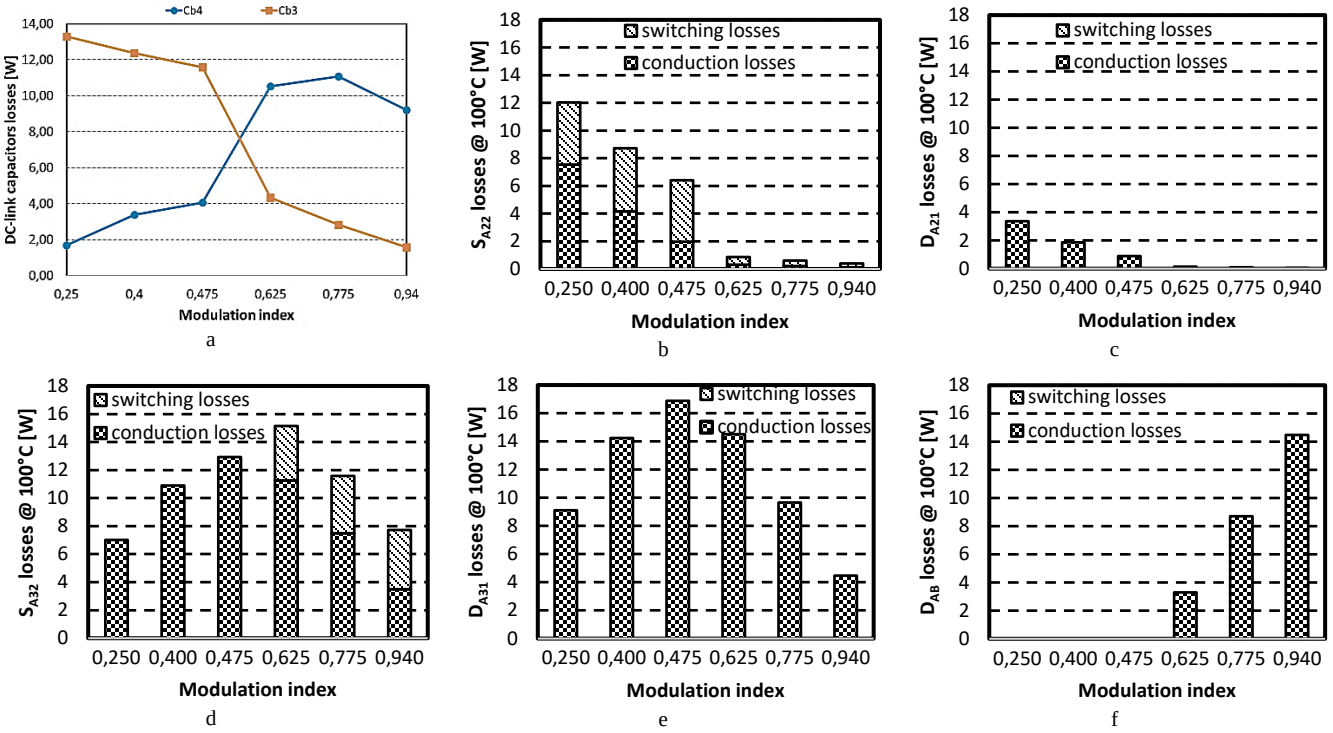

Figure 13. Power losses. a) DC-link capacitors; b) T-middle leg IGBTs S_{A22} and S_{A21}; c) T-middle leg diodes D_{A22} and D_{A21}; d) T-outer legs IGBTs S_{A32} and S_{A11}; e) T-outer legs diodes D_{A31} and D_{A12}; f) input rectifier diodes D_{AB} and D_{AA}

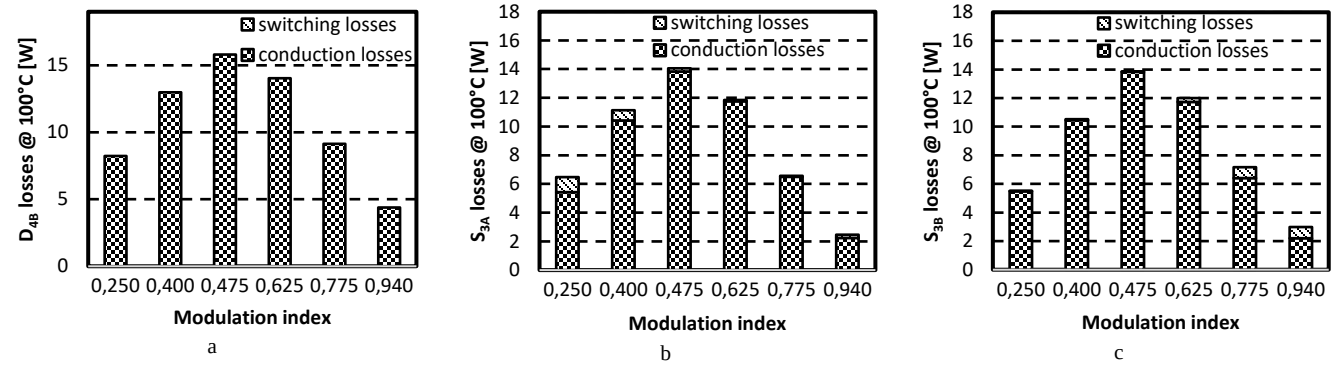

Figure 14. Balancing circuit power losses. a) outer diodes $D_{4A,B}$ and $D_{1A,B}$; b) inner IGBTs S_{3B} and S_{2A}; c) inner IGBTs S_{3A} and S_{2B}.

behaviors, power losses distribution in input rectifier diodes D_{AA} and D_{AB} is shown in Fig. 13f. Rectifier diodes start working for m_A higher than 0.5 with modulation index dependent increasing power losses.

Power losses of semiconductor devices in the resonant balancing circuit are depicted in Fig. 14. At steady state, the circuit symmetry allows to consider same behavior for the outer diodes as well for the IGBTs of the two inner legs in series connection. Both outer diodes and inner IGBTs exhibit the higher values of power losses when the converter modulation index m_A is close to 0.5.

With reference to Fig. 10, the losses related to the IGBT freewheeling diodes of the top-middle and bottom-middle legs have been omitted due to their negligible value. However, the diodes D_{A32} and D_{A11} are still necessary in the proposed configuration to avoid negative IGBT voltage during the commutation of the diodes D_{A31} and D_{A12}. According to that, the current rating of such diodes can be strongly reduced saving silicon and module area, thus reducing the cost of the proposed configuration.

VI. Experimental Results

A prototype of the 5L T-RECT with its own Resonant Balancing Circuit (RBC) has been built. Properly designed PCBs have been used for both the rectifier and its balancing circuit in order to reduce the parasitic inductances. Fig. 15 and Fig. 16 show respectively the rectifier prototype and the RBC realization.

As first experimental test, the 5L T-RECT has been loaded by a pure resistive load. The DC-link voltage was properly controlled at 700 V through a dedicated outer voltage loop. Generator torque and flux were regulated by a classical vector control scheme based on two proportional-

integral controllers. Current reference for d-axis was set to zero. The selected resistive load measures 36Ω and the experimental operating conditions result in the rated value for the line current, as listed in Table I.

Generator speed was set to 12000 rpm, to fully exploit all the five levels of the proposed AC-DC converter; as a consequence, the PMSG phase EMF measures 216Vrms. Resulting main waveforms are shown in Fig. 17. With reference to Fig. 3, Fig. 18 illustrates respectively the voltages between the Middle point, the Top-Middle point and the Bottom-Middle point, achieved with respect to the AC-DC phase A terminal. It can be noticed in Fig. 18a, that the maximum voltage between the Middle point and the phase A is equal to half DC-link, as previously illustrated in the theoretical section of the paper. This value can be used to select the voltage rating of the switches S_{A22} and S_{A21} and the diodes D_{A22} and D_{A21}. Fig. 18b depicts the Top-Middle to phase A terminal voltage, and it is applied to the series connection of switch and diode. When the switch S_{A32} is open, its voltage is ¼ V_{BUS} (negative part of V_{tm-a}); instead, when the diode D_{A31} is blocking, its voltage is ¾ V_{BUS} (positive part of V_{tm-a}). Fig. 18c is complementary to Fig. 18b. It highlights the voltage measured from the Bottom-Middle point and phase A terminal.

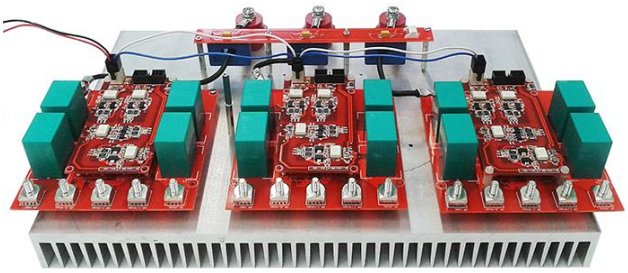

Figure 15. 5L T-RECT prototype.

Figure 16. Resonant Balancing Circuit PCB realization.

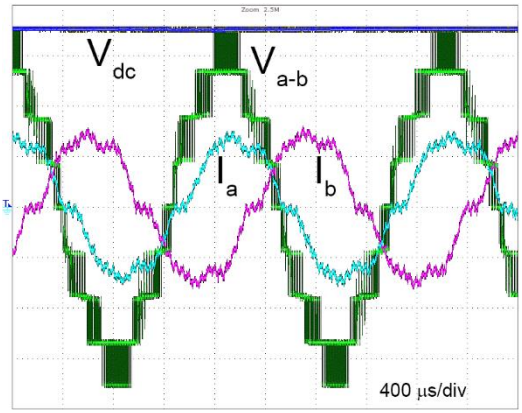

Figure 17. 5L T-RECT DC-link and line-to-line voltages and phase currents. Voltage (200 V/div), current (20 A/div).

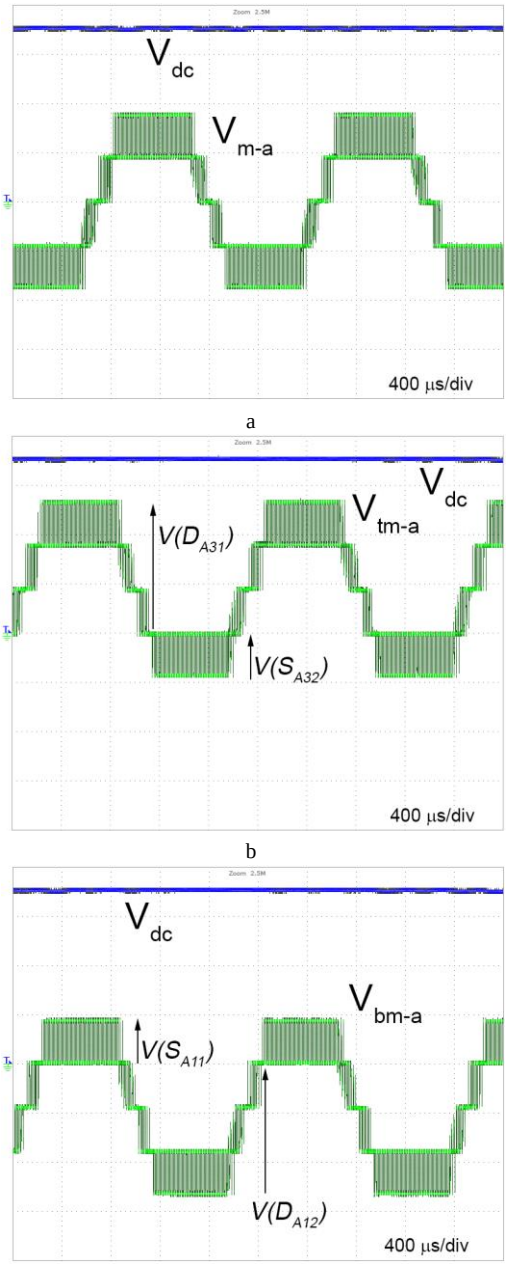

Figure 18. a) DC-link voltage (V_{dc}) and Middle point to phase A terminal voltage (V_{m-a}); b) DC-link voltage (V_{dc}) and Top-Middle point to phase A terminal voltage (V_{tm-a}); c) DC-link voltage (V_{dc}) and Bottom-Middle point to phase A terminal voltage (V_{bm-a}). Voltage (200 V/div).

In this case, the voltage across the switch S_{A11} is ¼ V_{BUS} (positive part of V_{bm-a}); whereas the diode D_{A12} inverse voltage is ¾ V_{BUS} (negative part of V_{bm-a}). Depicted experimental results confirm the theoretically evaluated voltage distribution across power components.

CONCLUSIONS

The proposed five-level unidirectional T-rectifier topology has been investigated in order to evaluate power losses and design criteria for switches and diodes of the three main sections of the configuration, the diode rectifier, the T section and the resonant balancing circuit. Suitable combination of high speed IGBT, SiC Schottky diodes and Si rapid switching diodes is used to manufacture the proposed configuration phase leg. The carried out analysis has shown very low total switching losses; further, the achieved power losses distribution among the devices as a function of the operating conditions provides useful information for improving the design and implementation of the T-rectifier phase leg. The achieved experimental waveforms validate the theoretical assumptions on voltage distribution across switches and diodes.

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