Digital Dead-Beat and Repetitive Combined Control for Stand-Alone Four-Leg VSI

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***Abstract* –This paper deals with a newly conceived combined control topology. Dead-Beat and Repetitive controllers are proposed to operate jointly in a 4-leg VSI for stand-alone applications. In such mode of operation, dedicated controller has to regulate the inverter output voltages, which are measured at the output of the power filter. In the proposed combined control, the Dead-Beat rapidly compensates the output voltage variations due to load changes; whereas, the Repetitive Control provides the required harmonic compensation capabilities that are mandatory to comply with the Standards, when balanced and unbalanced non-linear loads have to be fed. As a consequence, high dynamic performance is assured, as well harmonics in the output voltages are almost absent. In fact, the achieved experimental tests have verified that resulting output voltage THD is around 0.5% also in case of highly unbalanced and non-linear loads, compensating also the distortion introduced by the switches dead-time.**

I. Introduction

The reduction of the harmonic content of current and voltage waveforms at the output of power electronic converters is of increasing interest for today's applications, with particular reference to either Distributed Generation Systems or Uninterruptible Power Supplies or active filtering, which have to comply with severe Standards. The European Standards EN-50160 and EMC EN-61000 address the power quality limits that the utilities must satisfy; however, even if the European Union has its own regulation, each country can demand for mandatory requirements that are more restrictive. In case of main grid connected utilities, the EN-50160 considers the voltage Total Harmonic Distortion (THD_V) up to the 25^{th} harmonic with respect to the fundamental component. On the other hand, when stand-alone power generating systems are considered, the reference Standard for Uninterruptable Power Supply (UPS) equipment is the IEC 62040-3, which designates that, under specific linear and non-linear load conditions, the harmonic content of the output voltages should be within the IEC 61000-2-2 limits.

The application, to which the investigated combined control strategy addresses, relates to a 3-phase 4-wire power supply unit for AC stand-alone loads, which is formed by a 4-leg VSI and its dedicated output power filter. The conceived unit and its control have to be able to support a 3ph+n isolated grid in order to provide power supply to linear and non-linear loads, with either leading or lagging power factor.

Several control strategies have been investigated in previous works related to the output voltage regulation of the considered 4-leg inverter. In [1], a multi-resonant control approach was first proposed. It ensures a great flexibility of tuning gain and phase of each resonant controller at specific voltage harmonic points, though the hardware implementation and computing requirement was an issue. In order to overcome that, a resonant + repetitive solution was developed in [2]. The effort of the resonant controller was to provide the fundamental component tracking, and the use of the plug-in type repetitive controller was to compensate for all the harmonics. In spite of the fast dynamic performance and wide stability range, the high order harmonic compensation capability of the VSI system, under non-linear load condition, was compromised to some extent, mainly due to the filtering effort of the fundamental resonant controller. By considering the system is internally stable [3], [4], [5] demonstrated the direct repetitive control method, in order to further improve the output voltage quality. With the proposed load adaptive algorithm and the dedicated zero-phase-shift compensator for different load rating, the system was capable of providing an excellent output voltage even under highly non-linear load condition. However, the nature of the direct type repetitive control implies that an empty control cycle, i.e. no control action, is always required during the converter start-up, due to the absence of the conventional controller. In addition, an open loop control cycle is needed when a large load step change applies. This is potentially dangerous for critical electrical installations such as health care facilities, as the system stability cannot be assured during the open loop cycle.

With reference to the control aspects, this paper deals with a combined Dead-Beat and Repetitive controller (DB-RC) devoted to VSI output voltages regulation. The proposed parallel combination of Dead-Beat and Repetitive Control acts to fully exploit the benefit obtainable by each control structure when considered separately [6].

In this work, the Dead-Beat controller is designed to provide fast dynamic response during the system start-up or large load step changes, while the parallel type repetitive controller is employed to cope with the model uncertainties and load variations and hence to achieve high performances in steady state. A three-phase four-leg inverter prototype is utilized to verify the effectiveness of the proposed dead-bead and repetitive combined control algorithm.

Detailed description of the combined DB-RC structure is provided. Experimental tests have been conducted to highlight the combined action and to prove the benefits of the proposed control structure.

Classical Dead-Beat (DB) control was applied to single-phase stand-alone VSI in [7] highlighting its fast response to load variations. DB control is improved with prediction features in [8] where it was applied to DC-DC converters. Predictions capabilities of the Dead-Beat regulation are illustrated also in

[9] for AC-DC systems in grid-tied operation. However, DB structure is in general not able to provide harmonic compensation that is mandatory in off-grid application to comply with the standards.

On the other hand, Repetitive Control (RC) has been proved to the very effective to adjust periodic signals as disturbance harmonics [10]–[13]. Main drawback of the RC is represented by its inherent learning time, which reduces the overall dynamic performance, resulting in some cases in unacceptable compensation of load changes.

II. Converter Topology and System Description

In the last decade, many researchers of both industry and academia have addressed their studies to inverter and filter topologies for either grid-connected or stand-alone systems. In stand-alone configurations, topologies with neutral wire at the inverter power output become critical when extremely general-purpose loads require to be supplied. Many different types of load can be located in autonomous grids; as a result, the single-phase, multi-phase, linear and non-linear loads affect considerably the neutral wire current, which can be of significant amplitude as well quite distorted. Additional power losses and resonance phenomena can occur and result in faults in protection devices and electrical safety circuits. With reference to DC-AC conversion, two main topologies of power electronic converters with neutral wire are present in literature, the 3-phase 4-wire inverters with split DC bus capacitors and the 3-phase 4-leg inverters.

The 3-phase 4-leg inverter configuration makes use of an additional leg with respect to the conventional 3-phase topology as it is shown in Figure 1. The additional leg requires 2 more switches and power diodes as well extra driving circuits and higher complexity in modulation techniques and control strategies. In spite of this, the 4-leg inverter, when properly modulated, can assure the efficient regulation of the output phase voltage also in case of unbalanced and distorted loads. Modulation with injection of the 3rd harmonic as well SVM techniques are possible without affecting the harmonic content in the phase-to-neutral voltage; further, the neutral current flows through the added leg and no oversizing is required for the DC-link capacitors. Prototypal realization of a 3-phase 4-leg inverter as shown in Figure 2 is used to experimentally investigate the DB-RC combined control. The prototype characteristics are listed in Table I.

TABLE I - 3-Phase 4-Leg Inverter Prototype Main Characteristics

Rated Power	40kVA
Line-to-Line Voltage	400±10% V
Switching Frequency	12kHz
Efficiency @ rated power (output filter included)	0.97
Power Modules	Semikron - SEMIX303GB12Vs
DC-Link Capacitors	MKP 3 x 150µF – 900Vdc
AC Output Inductors	800 µH
AC Output Main Capacitors	MKP 5µF – 480Vac
Control Board	TI-TMS320F28335

Power inverter is modeled through its first order approximation, which is very simple to manage. The inverter is seen, from the control algorithm, mainly as a gain with a delay due to the discretization caused by the PWM unit as it is shown in (1), where K_m is the gain depending to the modulation strategy, V_{dc} and F_{sw} are respectively the DC-link voltage and the inverter switching frequency. Acquired phase voltages are filtered by means of a second order low-pass Butterworth filter having the transfer function as in (2), where ω_f is the filter cut-off frequency.

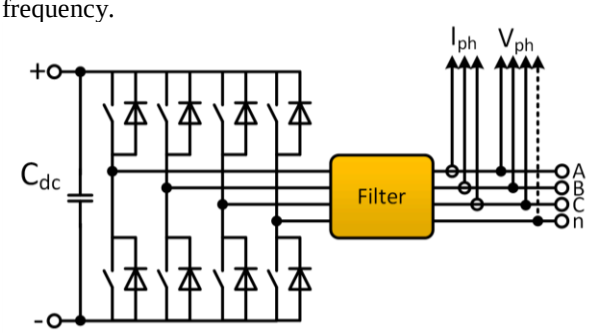


Figure 1. 3-Phase 4-Leg Inverter.

$$G_{4-leg}(s) = \frac{K_m V_{dc}}{1 + \frac{s}{2\pi F_{sw}}} \quad (1)$$

$$G_{lpf}(s) = \left(\frac{\omega^2_f}{s^2 + \sqrt{2}\omega_f s + \omega^2_f} \right) \quad (2)$$

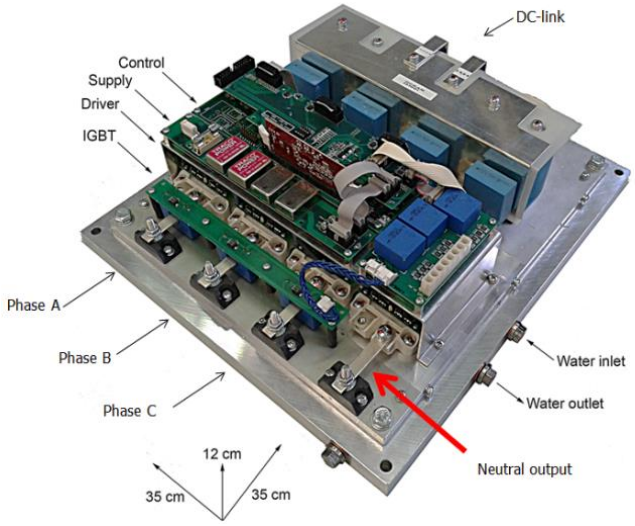


Figure 2. 3-Phase 4-Leg Inverter Prototype.

Inverter output filters are necessary to remove the switching components from the output voltages and currents. In the present study, it is considered the single-phase equivalent filter structure as shown in Figure 3, where the conventional LC second order main filter is connected to two tuned RLC branches: the trap-filter and the selective damper [14]. The selective damper is centered at the frequency of about 20% higher than the LC resonance frequency in order to damp the LC resonance peak, making the R_d resistor visible to the rest of the circuit only in a restricted range of frequencies. The trap-filter is instead tuned to resonate at the switching frequency (R_t is the sum of L_t and C_t ESRs), in order to short-circuit the switching fundamental component. Filter transfer function can be simply achieved considering the impedance of each part of the filter in the s-domain as in (3) without the load connected at the filter output.

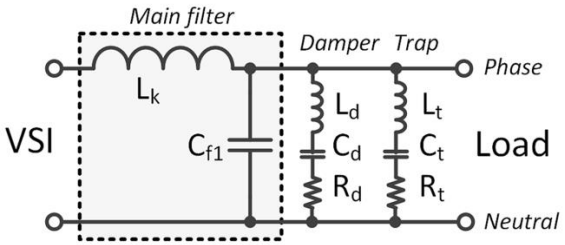


Figure 3. Scheme of the considered output power filter.

$$Z_{trap}(s) = sL_t + \frac{1}{sC_t} + R_t\,,\ Z_{dump}(s) = sL_d + \frac{1}{sC_d} + R_d\,,$$

$$G_{pwf}(s) = \frac{Z_{dump}(s)\,//\,Z_{trap}(s)\,//\,\dfrac{1}{sC_{f1}}}{sL_k + \left(Z_{dump}(s)\,//\,Z_{trap}(s)\,//\,\dfrac{1}{sC_{f1}} \right)} \qquad (3)$$

III. Dead-Beat + Repetitive Combined Control Strategy

For the proposed four-leg VSI system, the fourth leg is utilized to provide a neutral connection, and it is modulated without direct voltage regulation as suggested in [15]. Hence, from the control point of view, the three-phase system can be de-coupled and each phase can be considered separately as a standard single-phase inverter. As a result, individual digital control loop can be applied to regulate the three phase-to-neutral voltages.

A. Proposed DB + RC Control Strategy

Taking all the aforementioned limitation into account, a novel parallel type dead-beat (DB) + repetitive (RC) control strategy is proposed for the system output voltage regulation. Figure 4 shows a generalized control block diagram of each phase, where $G_{4\text{-}leg}(s)$, $G_{pwf}(s)$ and $G_{lpf}(s)$ represent the 4-leg VSI, the power filter, and the measurement low pass filter, respectively as given in (1), (2) and (3).

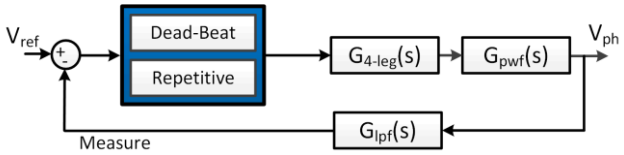


Figure 4. Generalized control block diagram of each phase.

In this work, the Dead-Beat controller is designed to provide fast dynamic response during the system start-up or large load step changes, while the parallel type repetitive controller is employed to cope with the model uncertainties and load variations and hence to achieve a high performance in steady state. Detailed design procedures are presented in the following sub-sections.

B. Dead-Beat Control Design

Owing to its high control bandwidth feature, Dead-Beat control has been considered widely for digital implementations demanding fast dynamic response. For linear time-invariant (LTI) systems, it is capable of finding an actuating signal to bring the output to the steady state in the smallest number of time steps. The main drawback of the Dead-Beat controller is the high sensitivity to model uncertainties, parameter mismatches, and measurement noises. Since it is based on pole-zero cancellation, a good knowledge of the target plant is normally required. Otherwise, the control performance is reduced in presence of unpredicted disturbances such as dead-times, as there is no inherent integral action involved [16].

1) Pole-Zero Movement

Since a wide load range operation is demanded for this application, the system plant is analyzed under different load conditions (linear load varying from 350W to 6kW per phase). Figure 5 presents the corresponding pole-zero movement in the discretized domain, in order to highlight the load influence on the system pole-zero distribution.

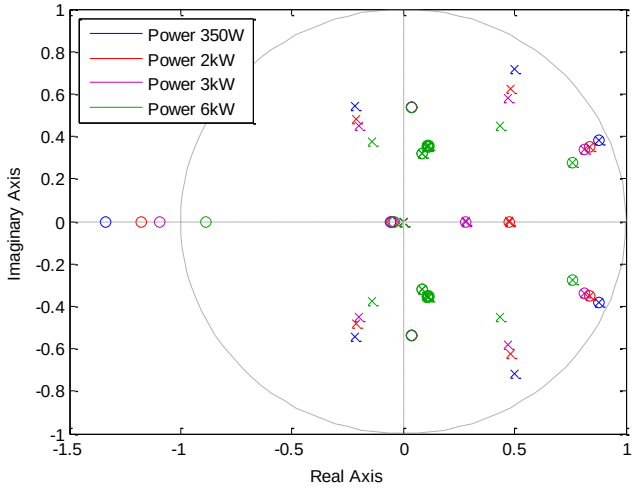


Figure 5. Pole-zero movement of the system plant under different load conditions (linear load varying from 350W to 6kW per phase).

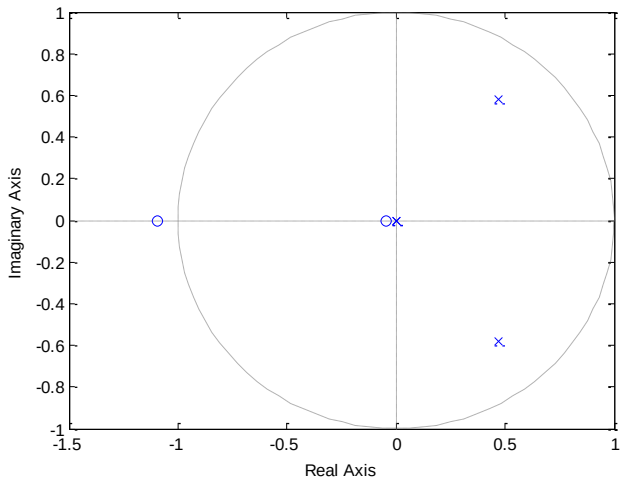
As it can clearly observed that, from the right hand side of the unit circle, a pair of low frequency poles is always cancelled by associated zero pair, for all different load conditions. Hence, their effects can be neglected. Similar pole-zero cancellations also occur in the central zone of the unit circle, which can be ignored as well during the control design phase.

When the converter is loaded with 350W linear load, it has one zero outside the unit circle, one pair of complex poles locating at the low frequency band (0.49±0.72i), and one pair of complex poles at the high frequency band (-0.22±0.55i). When the output power increases, the poles approach towards the central zone, while the zero moves into the unit circle. Generally speaking, the system is internal stable, and tends to be more stable when the load power increases.

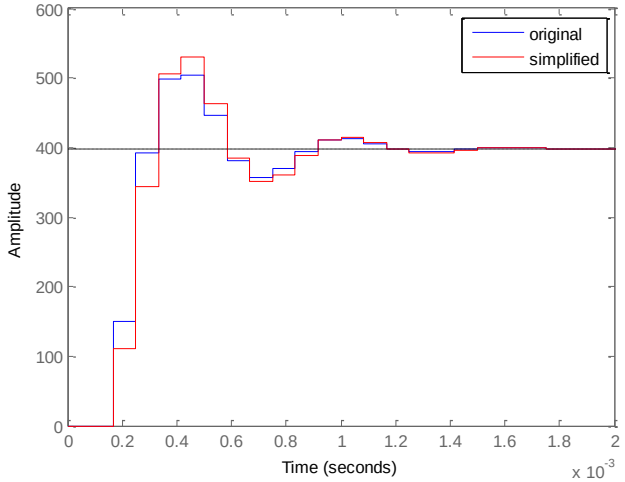
2) Simplified Plant

For this application, the dead-beat control design is inherently difficult, due to the following reasons: first, the wide load rang requirement implies that the dead-beat controller need to cope with different pole-zero distribution, which makes a perfect cancellation is impossible; second, the pole/zero mismatches between the plant and designed dead-beat controller would introduce high frequency poles, which makes the whole control system more sensitive to noises and disturbances.

In this work, since the dead-beat controller is employed only to provide fast dynamic response during the system start-up or large load step changes, a simplified plant is introduced by considering only the dominant low frequency dominant poles and zeros. Considering a one-unit delay (1/z) representing hardware sampling and modulation time, the pole-zero map and the step response of the simplified plant are shown in Figure 6. As it can be seen, the dynamic of the simplified plant is very close to that of the original.



(a)



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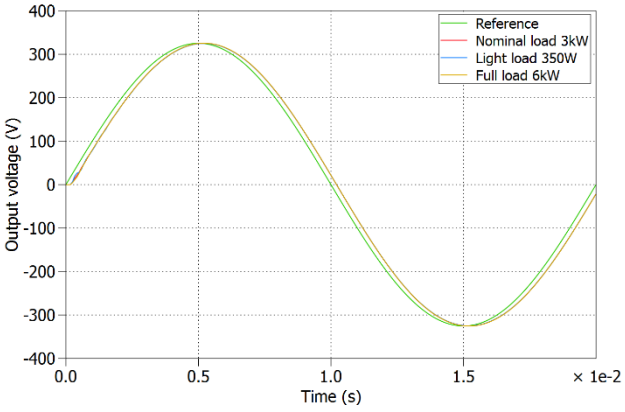

(c)

Figure 6. (a) pole-zero map on the simplified plant; (b) step response comparison of the original plant and simplified plant; (c) closed loop responses with the designed dead-beat controller under 350W, 3kW and 6kW.

Based on it, the complete dead-beat controller can be designed and expressed as in (4).

$$G_{DBC}(z)=\frac{z^4-0.94z^3+0.56z^2-0.001z}{233z^4+11.2z^3-111.3z^2-127.1z+5.84} \quad (4)$$

The use of this simplified plant brings several benefits for the whole control system: first, it leads to a simple dead-beat control structure for easy hardware implementation; second, the relatively straightforward dead-beat control loop relieves the complexity of the following repetitive control design; third, it avoids introducing the high frequency poles and zeros of the dead-beat controller, which makes the whole control system less sensitive to the load variations during transient performance.

In order to verify that the designed dead-beat controller is the stable for the full load range, Figure 6 (c) presents the comparison of the closed loop responses with the nominated load 3kW (red), light load 350W (blue), and full load 6kW (yellow), respectively. As it can be seen, the system is sufficiently stable for the whole load condition, and the three curves overlap each other (only slight transient discrepancy at the beginning). It is worth to note that, although the system stability can be assured, the use of this dead-beat controller imposes a considerable phase error in steady state. A parallel type repetitive controller is introduced to achieve a high performance in steady state.

C. Parallel Type Repetitive Control Design

Repetitive control attracts more and more interests in modern industrial applications for feedback systems that are subject to periodic reference inputs or periodic disturbances. Based on the internal model principle (IMP) [17], the repetitive controller processes the error signal of the previous period and applies the resultant signal to improve the control performance of the current cycle. Theoretically, with a suitably designed repetitive controller, the output of a stable feedback system can track the periodic reference signal or/and reject the exogenous periodic disturbance with zero steady state error even in the presence of model uncertainties.

1) RC Structure

Figure 7 shows the detailed structure of the parallel repetitive controller, where k_{RC} is the repetitive learning gain, z^{-N} is the delay line, $Q(z)$ is the robustness filter, and $G_f(z)$ is the stability filter. N is the ratio between the period time of the reference and the digital sampling time. The use of the robustness filter $Q(z)$ is to modify the internal model, which effectively increases the system stability margin.

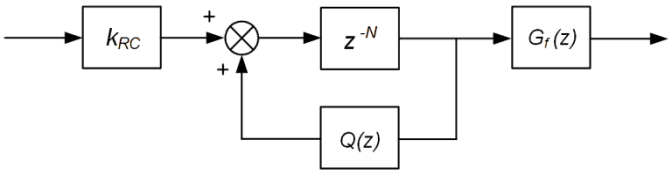

Figure 7. Detailed structure of the parallel repetitive controller.

Considering the wide load range operation, a moving average filter of $0.25z^2+0.5z+0.25/z$ has been selected in this work, in order to improve the whole system stability at high frequency

band. The design of k_{RC} and $G_f(z)$ is coupled and is also correlated with the selection of $Q(z)$.

2) Stability Analysis

According to the small gain theorem [15], two sufficient stability conditions for the parallel RC system can be summarized as follows: (a) the control system (without the parallel RC) is inherently stable; (b) equation (5) is guaranteed for all the frequencies below the Nyquist frequency ω_{nyq}, where G_P is the system plant transfer function.

$$\left| Q(e^{j\omega T_S}) - \frac{k_{RC}\, G_f(e^{j\omega T_S}) G_P(e^{j\omega T_S})}{1 + G_{DBC}(e^{j\omega T_S}) G_P(e^{j\omega T_S})} \right| < 1 \qquad (5)$$

The first condition can be guaranteed, as the Dead-Beat controller has been properly designed. The second one can be proved by examining the Nyquist locus curve of equation (5). A ninth order low pass filter is proposed, based on the design approach discussed in [3], as stability filter G_f, in order to ensure equation (5) is always guaranteed for the whole operating range of the VSI inverter system.

Figure 12 shows the Nyquist locus curve of equation (5) with G_f (z) implemented under 350W, 3kW and 6kW linear load, respectively. Clearly, the magnitude stays within in the unitary circle for the whole load range, which proves that the overall control system is adequately stable.

3) Design Result

Table II summarizes the design result of the repetitive controller. The delay chain is achieved by the ratio between the algorithm sampling frequency and the fundamental harmonic to track. It this case 12kHz divided by 50Hz.

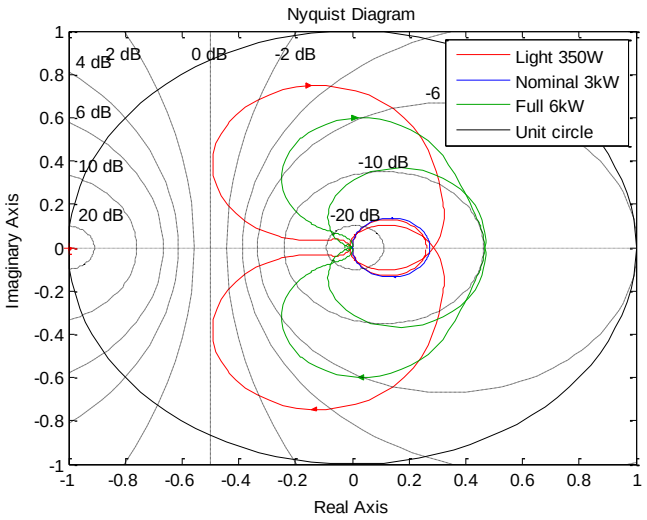

Figure 12. Nyquist locus curve of equation (5) with G_f (z) and k_{RC} of 0.2 under 350W, 3 Kw and 6kW linear load, respectively.

TABLE II - REPETITIVE CONTROLLER DESIGN RESULT

Symbol	Description	Value
N	Delay chain	240
k_{RC}	Repetitive learning gain	0.2
$Q(z)$	Robustness filter	$0.25z^2+0.5z+0.25/z$

IV. SIMULATION AND EXPERIMENTAL RESULTS

Figure 8 shows the voltage reference and the output voltage of Phase A during the system start-up, when a 3kW linear load is applied on each phase. As it can be seen, a very good tracking is achieved, due to the effort of the designed Dead-Beat controller, though a slight delay, which is approximately equal to two sampling delays, can be observed between the voltage reference (red trace) and the output voltage (green trace). At the

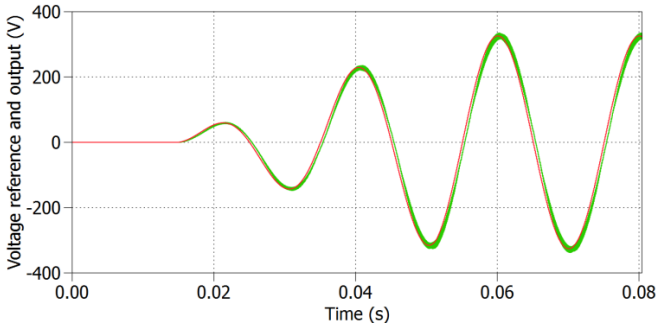

Figure 8. Voltage reference and output voltage of Phase A during system start-up, with 3kW linear load per phase.

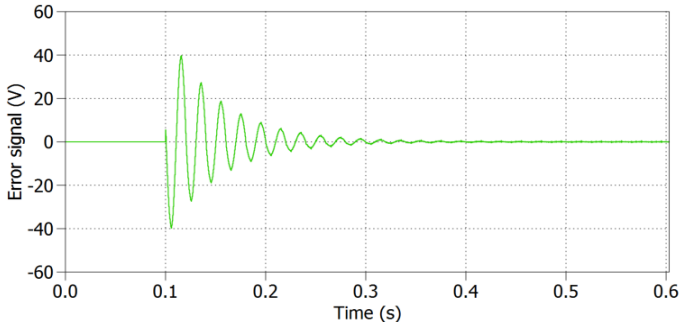

Figure 9. Voltage error signal of Phase A seen by the repetitive controller.

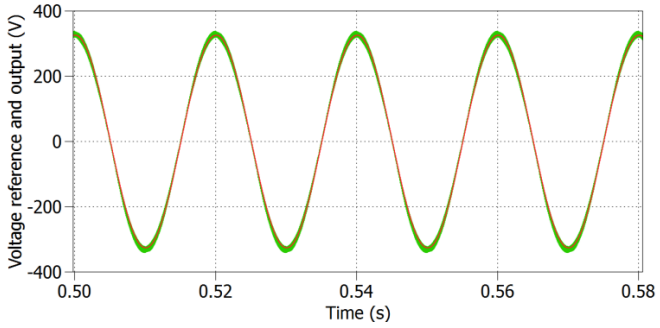

Figure 10. Voltage reference and output voltage of Phase A in steady state, with 3kW linear load per phase.

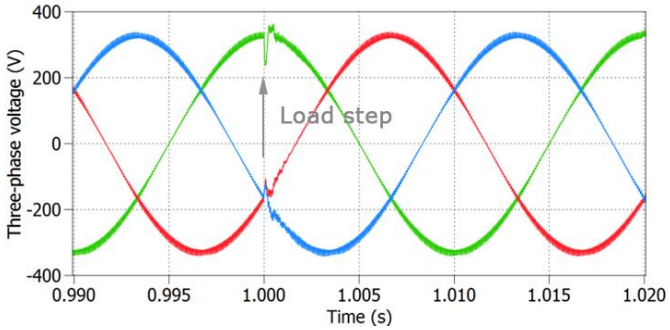

Figure 11. Three-phase output voltage during load step change, from 3kW to 6kW occurring at 1 s.

time point of 0.1 s, the parallel type repetitive controller has been enabled. As shown in Figure 9, the periodic error signal starts to converge very quickly to a very small level (less than 1 V), and whole system is firmly stable. Figure 10 presents the voltage reference and the output voltage of Phase A in the steady state mode of operation. A large load step change test is then applied to examine the system control performance.

At the time point of 1 s, the load is changed from 3kW to 6kW. Figure 11 highlights the corresponding three-phase output voltage. It can be noted that the system is firmly stable and the error converges quickly for the large load step change.

The inverter prototype shown in Figure 2 has been used for the experimental tests to validate the illustrated control strategy. Proposed DB-RC has been implemented on the TMS320F28335 DSP from Texas Instruments, which is assembled on a dedicated board. Single-precision 32-bit floating-point numeric representation has been used for both the Dead-Beat and the Repetitive controls.

At first, DB-RC is tested in the no-load condition to demonstrate the correct operation being the inverter output filter response completely undamped. Phase voltages and currents are highlighted in Figure 13 where a good regulation is obtained. Additionally, a 3-phase linear balanced load test has been performed where each phase was loaded by 4kW resistive rack. It can be noticed from Figure 14 that the load-side voltages exhibit a very low THD with negligible dead-time distortion.

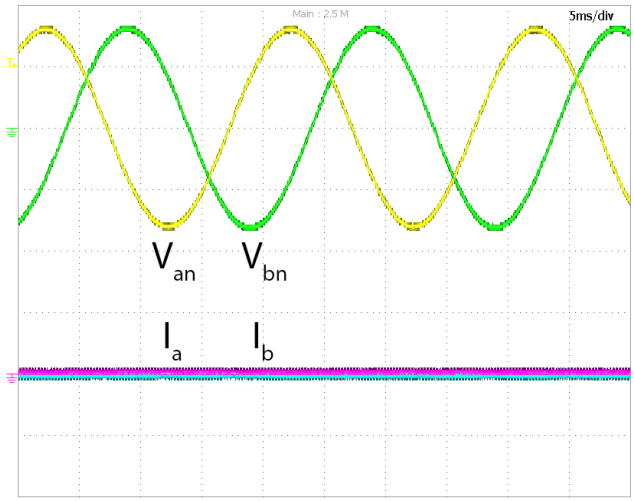

Figure 13. Experimental results under no load conditions, undamped condition. (Voltage 200V/div).

Steady-state control behavior is shown also when non-linear loads have to be fed. Non-linear load configuration is illustrated in Figure 15. In the case shown in Figure 16 a single-phase diode rectifier is connected to the output of the VSI power filter. Phases B and C are at no-load condition. It can be recognized the near-zero voltage distortion that is achieved mainly because of the Repetitive part of the proposed controller. A similar test has been performed using a single-phase non-linear load, which was directly connected between phase A and the neutral wire, performing a load step test to validate the Dead-Beat parallel controller.

Results are shown in Figure 17, where the validity of the proposed controller can be documented looking to the V_{an} and V_{bn} voltages. Also in this case, voltage drop is within the maximum allowed by the standard being less than 12V (~3.8%), due to the DB control and its characteristics that are fully exploited. The benefits of the DB action can be recognized by comparing the result obtained in Figure 17 when both the controllers are engaged, with the load step behavior obtained where only the Repetitive Control is operating as shown in Figure 18. It can be clearly noticed the relevant phase voltage drop as well as the longer time required to compensate it. Experimental results during continuous ON-OFF single-phase non-linear load are reported in Figure 19 where the phase voltage limits are also superimposed to highlight the regulation capability of the proposed DB-RC structure.

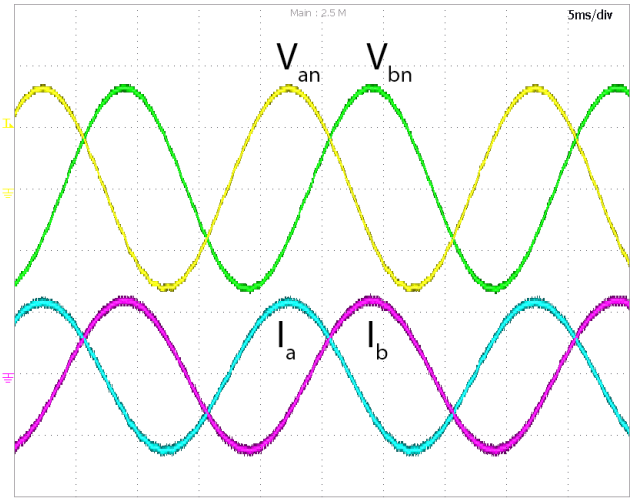

Figure 14. Experimental results under linear a 12kW balanced load, (Voltage 200V/div, Current 20A/div).

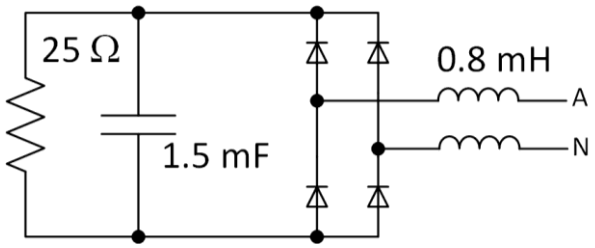

Figure 15. Single-phase non-linear load.

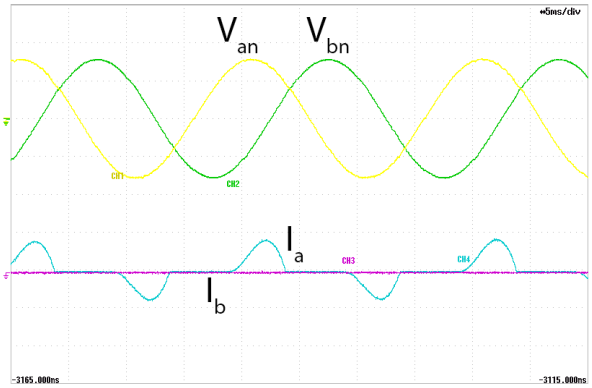

Figure 16. Steady-state behavior for single-phase non-linear load, ~4kW. (Voltage 200V/div, Current 50A/div).

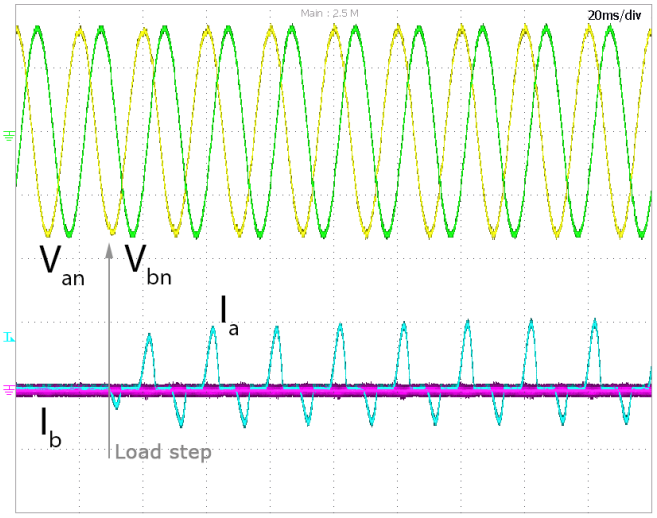

Figure 17. Single-phase non-linear load step test from 0kW to 4kW. (Voltage 200V/div, Current 50A/div).

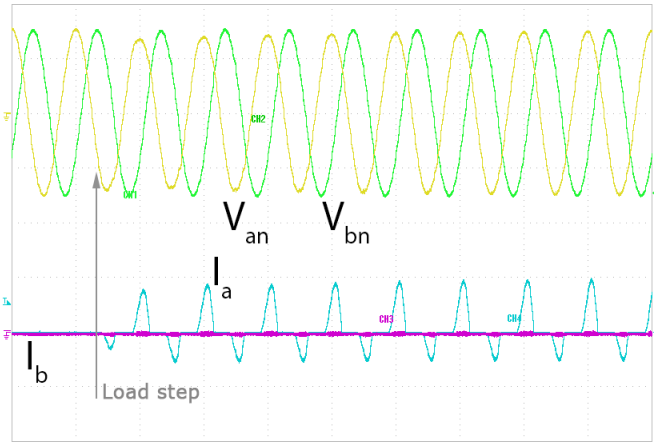

Figure 18. Single-phase non-linear load step test from 0kW to 4kW. (Voltage 200V/div, Current 50A/div), Repetitive Control only.

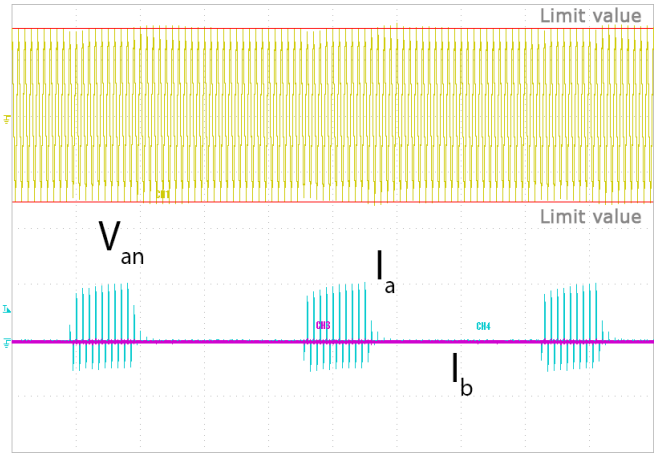

Figure 19. Single-phase repetitive non-linear load steps from 0kW to 4kW. (Voltage 200V/div, Current 50A/div).

When the single-phase diode rectifier load is fed, two effects arise. At first the AC power is not constant with the additional issue that the current has an important harmonic content. Even if the VSI is able to compensate the harmonics providing an output voltage waveform having a near-zero-THD, such a distortion is reflected on the input DC-link. Hence, the DC-bus voltage exhibits some oscillations. As a consequence, non-negligible current unbalance at the input of the diode rectifier can occurs. The DC-link voltage oscillations are more significant during transients than during steady state of operations; for this reason, the line current is quite unsymmetrical in Figures 17-19 and it is almost symmetrical in Figure 16.

A three-phase non-linear load implemented by the diode rectifier shown in Figure 20 has been used to verify the steady-state behavior of the proposed DB-RC structure. Results are highlighted in Figure 21, where it can be noticed how the RC action is capable to provide a near-zero THD for the output voltages. Moreover, the dead-time distortion which is mainly composed by 5^{th} and 7^{th} harmonics is completely compensated. This effect saves the implementation of a dedicated dead time compensating algorithm, thus making the whole control algorithm simpler and effective.

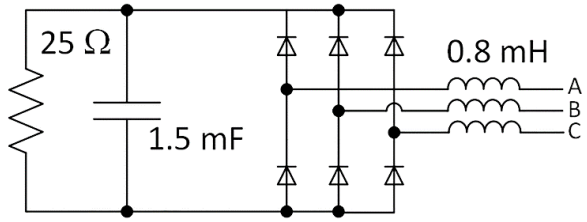

Figure 20. Three-phase non-linear load.

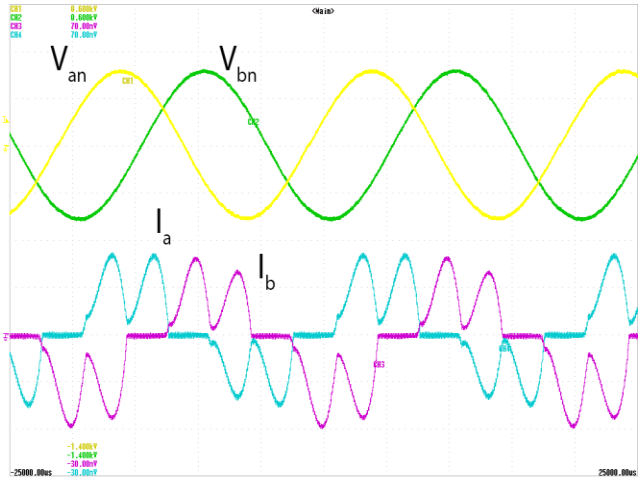

Figure 21. Steady-state behavior for three-phase non-linear load, ~13kW. (Voltage 200V/div, Current 20A/div).

In agreement to what was shown for the single-phase load, a load step test is performed using the previously described three-phase load arrangement. It has been suddenly connected to the output of the 4-leg inverter performing a no-load to ~13kW load step. Output voltages behavior and current waveforms are shown in Figure 22. It can be noticed that the voltage drop is very small thanks to the Dead-Beat control, even if the output voltages are strongly distorted due to the iterative learning action required by the Repetitive Control to fully compensate harmonics. Of course, as the transient phase is concluded in less than twelve periods of the fundamental harmonic, the voltage harmonics are fully compensated and same distortion as in Fig. 21 is achieved. Performance of the combined DB-RC control structure has been also tested by a sequential load variation with the 3-phase diode rectifier load. During the test, the load is periodically connected and disconnected to verify the

regulation quality. Results are illustrated in Figure 23, where it can be noticed the good output voltage regulation, being the under voltage and over voltage very low.

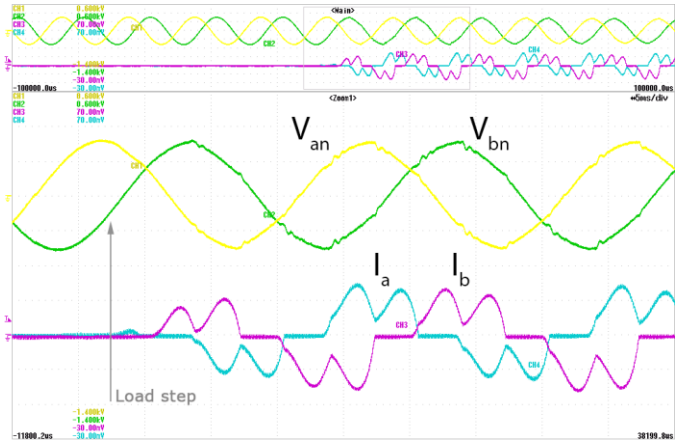

Figure 22. Three-phase non-linear load step test from 0kW to ~13kW. (Voltage 200V/div, Current 20A/div).

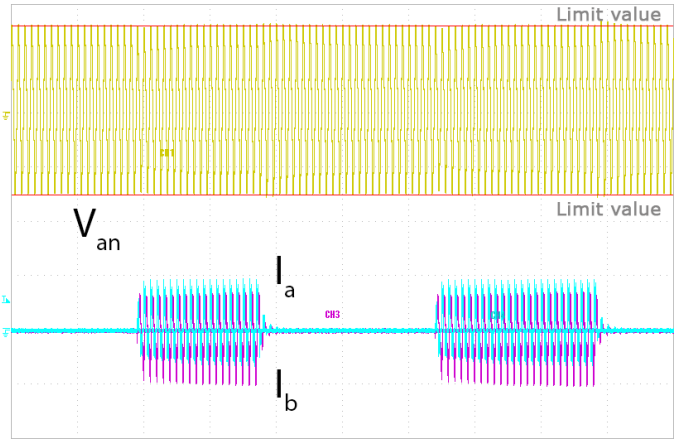

Figure 23. Three-phase non-linear load steps from 0kW to ~13kW. (Voltage 200V/div, Current 20A/div).

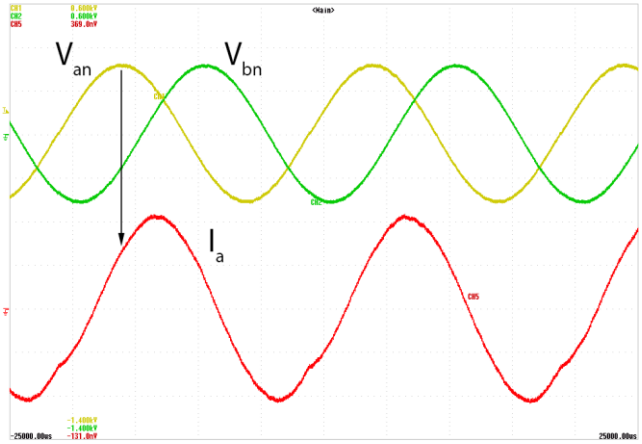

Figure 24. Steady-state phase voltages and phase A current when an induction machine is directly fed. (Voltage 200V/div, Current 20A/div).

Moreover, the combined DB-RC action has been tested using a load having a variable power factor lower than one, such as an induction machine. Results are reported in Figure 24, where it can be recognized how the control is perfectly stable and the output voltage is correctly regulated. Power factor is highlighted with a black arrow: phase A current is lagging phase A to neutral voltage.

Finally, the harmonic compensation capability of the combined DB-RC action has been evaluated through measurements of the harmonic content of the output phase voltage. Each frequency component has been measured by the PZ-4000 power meter from Yokogawa. Results are shown in Figure 25, where the amplitude of each harmonic is reported as percentage of the fundamental. Thanks, to the accurate harmonic regulation, the output voltage THD is almost independent of the load type. Measurements achieved by the power meters were absolutely identical, disregarding the type of load to be fed. The resulting output voltage THD was around 0.5% during all tests, compensating also the distortion introduced by the switches dead-time. This remarks the benefit of using the proposed Repetitive Control strategy to compensate the introduced output harmonics. Moreover, the illustrated parallel combined controller, takes the most from each specific algorithm. Same measurement procedure has been adopted to evaluate the output voltage harmonic content where a single-phase diode rectifier load is fed by the 4-leg VSI. Results are illustrated in Figure 26 with reference to the phase A, which is the inverter phase being under load condition. It can be noticed that the output voltage harmonic content is almost independent by the load to be supplied, highlighting the benefits in using the proposed control strategy.

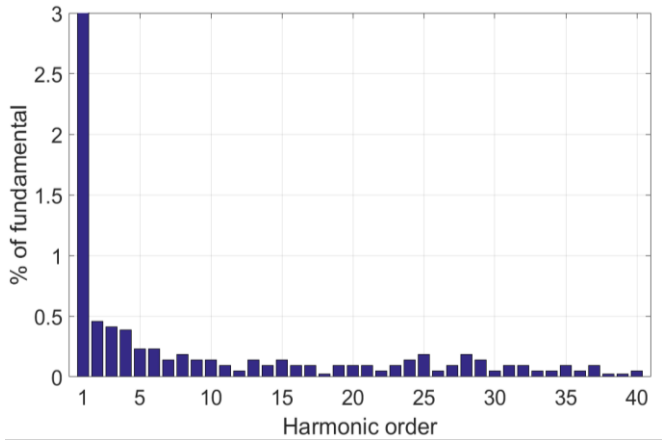

Figure 25. Harmonic content of the output phase voltage resulting from the three-phase diode rectifier load.

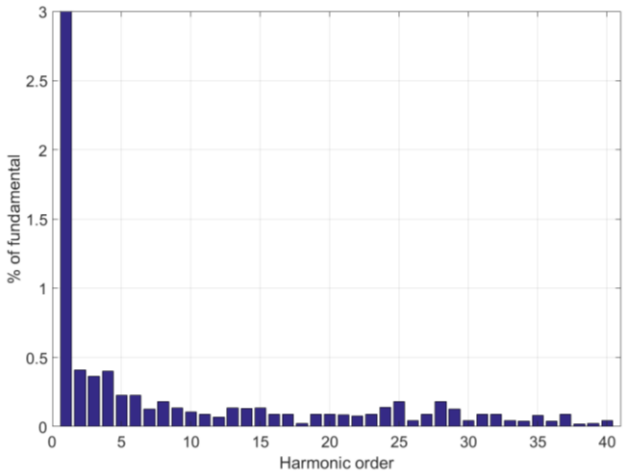

Figure 26. Harmonic content of the output phase A voltage resulting from the single-phase diode rectifier load.

CONCLUSIONS

The combined control action provided by the digital Dead-Beat and the Repetitive controllers is proposed and tested. DB-RC resulting controller is being able to take characteristic benefits of each of the two control strategies. DB acts primarily to compensate load variations, whereas RC provides the necessary harmonic regulation. Illustrated experimental results performed both in steady-state and transient conditions were used to emphasize the control action of either the Repetitive Control or the Dead-Beat algorithm. The resulting output voltage THD is around 0.5% also in case of highly unbalanced and non-linear loads, compensating also the distortion introduced by the switches dead-time. The achieved results show that the proposed combined control action is able to fully exploit the specific characteristics of each structure, making the 3-ph 4-leg inverter with the DB-RC an ideal candidate to supply sensitive loads in UPS as well as in micro-grid applications.

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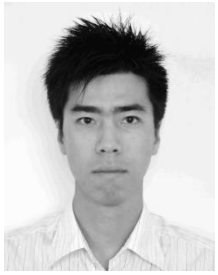

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