Five-Level E-Type Inverter for Grid-Connected Applications

Marco di Benedetto, *Member, IEEE,* Alessandro Lidozzi, *Member, IEEE,*
Luca Solero, *Member, IEEE,* Fabio Crescimbini, *Member, IEEE,* Petar J. Grbovic, *Senior Member, IEEE.*

***Abstract*– Nowadays, multilevel converter represents a good idea for commercial and industrial applications, where small size and cost, low maintenance, reliability in a wide range of environments and good efficiency are required. Furthermore, the multilevel converter can provide control for both maximum power tracking and output power factor reducing the filter weight and volume. The proposed power converter topology, called Five-Level E Type Inverter (5L E-Type Inverter), for grid connected applications is presented and analyzed in this paper. The performance of the three-phase 5L E-Type Inverter has been theoretically investigated. The thermal models of the power semiconductor have been created taking into account the parameters provided by the manufactures and employing multi-dimensional look-up tables in Plexim/PLECS environment. The design and selection of passive components have been described in order to obtain amazing performances in terms of weight, volume and efficiency and power quality. New control strategy, named concurrent control, for 5L E-Type Inverter has been implemented and validated in LabVIEW development environment. The peak efficiency of the converter above 98.3% and the total harmonic total harmonic distortion current (THD_i) less than 3% have been achieved.**

Keywords— DC-AC power conversion, multilevel converter, harmonic distortion, modulation, high-efficiency.

I. INTRODUCTION

The power electronics target is to reduce as much as possible the costs, size, weight and losses of the conversion systems and increase the power quality [1], [2]. To reach this purpose, new material processing and fabrication techniques, power devices, packaging and drivers have been developed and are still under investigation [3], [4]. In parallel with the power semiconductor evolution, new converter topologies and new control platform technology will play an important role in continuous efficiency improvement, power density, power quality and cost reduction. One way to achieve the mentioned targets is to deploy multi-level and/or multi-cell power converter topologies [1], [5]-[12]. It is true, as the working number of voltage levels of the converters increases, multilevel converters greatly increase the number of power devices. As a result, use more power semiconductors can be disadvantageous. From a material point of view, the power semiconductors are nothing else than a piece of roosted sand. Raw material is basically sand and it is 27% of the planet. This means that we have a lot of material. In contrast to this, inductor, transformers and capacitors are very dirty technology due to the use of iron, copper and aluminum; they are limited raw material. Having all this in mind, it is obvious that the only solution for future development is to use more and more power semiconductors and less iron and copper. In fact, applications linked to the power semiconductors have had a cost reduction in the recent years. Furthermore, iron and copper, which are the basic materials for the manufacture of inductors and transformers, are not cheap at all. Thus, from a cost point of view, if the number of semiconductor devices increases in a power converter, it does not mean that the cost of the overall system becomes higher. Additionally, the multilevel converter's success can be highlighted as the higher voltage operating capability, lower common-mode voltages, reduced voltage derivatives (*dv/dt*), voltages with reduced harmonic contents, near sinusoidal currents, smaller input and output filters, increased efficiency [5]-[12] and, in some cases, possible fault-tolerant operation [13], [14]. The use of a high number of power devices requires monitoring methods and fault indicators in order to have a safe and functional power conversion systems [13], [14]. An interesting investigation on the fault tolerance analysis has been addressed in [14] with reference to multilevel converter named 5-level Unidirectional T-Rectifier. In this paper, three phase 5L E-Type Inverter (3Φ5L E-Type Inverter) has been investigated and analyzed in order to obtain high efficiency, high power density and power quality to be used in grid-connected applications. Three-phase four wire equivalent circuit diagram of the solution under consideration is shown in Fig. 1.

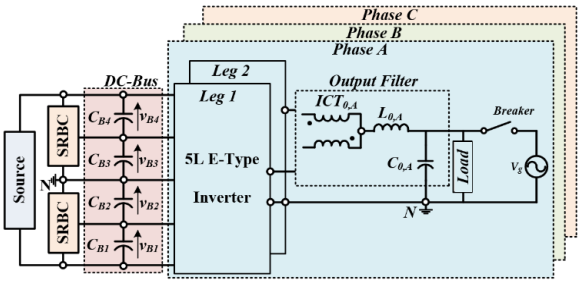


Fig. 1. Block diagram of the grid-connected interleaved 3Φ5L E-Type Inverter.

The performance of the interleaved 3Φ5L E-Type Inverter has been investigated using Plexim/PLECS tool in the Matlab/Simulink environment. The output filter, Inter-Cell Transformer (ICT_0), L_0 and C_0, has been designed in order to achieve THD_i <3%. Furthermore, the inverter control strategy, called concurrent control, has been implemented using the multi-resonant controller [15]. In this control strategy, the source feeds the local loads, even when the grid is disconnected from the system, allowing to meet the intentional islanding operation [16], [17], [18]. Consequently, the concurrent control has two operating mode: grid-tied mode and islanding mode. According to the proposed control strategy, the power quality international standards, such as IEEE STD 519-2014, EN 50160 and IEC 61000-2-4, are widely met.

II. 5L E-TYPE INVERTER TOPOLOGY

As it can be seen from Fig. 1, the DC-bus capacitors of the 3Φ5L E-Type Inverter is connected to the source through the two-voltage balancing circuit [7], [8], [12], [19]. The voltage balancing devices are used in order to obtain four equal voltage across the series connected capacitors [11]. The balancing converter can be considered as a series resonant converter (Series Resonant Balancing Circuit - SRBC) that operates in discontinuous conduction mode (DCM), type 1 [12], [19]. For simplicity in the following analysis, the DC-bus partial voltages v_{CB1}, v_{CB2}, v_{CB3} and v_{CB4}, are assumed to be equal to $¼V_{BUS}$, where V_{BUS} is the total DC-bus voltage. Each phase (*A*, *B*, *C*) consist of two 5L T-type Inverter legs (leg 1, and leg 2) connected in parallel through the magnetic coupling device (Inter-cell Transformer, ICT). Besides the $ICT_{0,x}$, with x∈{ *A*, *B*, *C*}, the output filter consist of the output inductor $L_{0,x}$ and the output capacitor $C_{0,x}$. The single leg 5L E-Type Inverter is shown in Fig. 2.

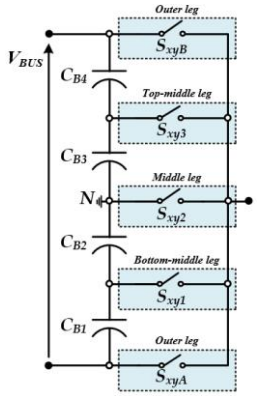
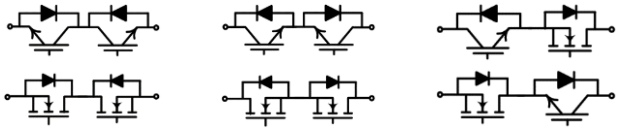


Fig. 2. Single leg 5L E-Type Inverter.

The switches situated in the outer legs S_{xyA}, S_{xyB}, with x∈{*A*, *B*, *C*} and y∈{*1*, *2*}, are voltage unidirectional and current bidirectional. The switches located in the top-middle, middle and bottom-middle leg, S_{xy3}, S_{xy2} and S_{xy1}, are voltage and current bidirectional. Thus, the switches S_{xy1}, S_{xy2} and S_{xy3} can be created by connecting two unidirectional switches IGBT or MOSFET in Common Collector (CC) or in Common Emitter CE (or common drain), as shown in Fig. 3. Additionally, it possible realize a hybrid configuration by connecting a mixed combination of both IGBT and MOSFET.



(a) (b) (c)

Fig. 3. Possible configuration of switches: a) bidirectional switches in CC, b) bidirectional switches in CE, c) hybrid bidirectional switches in CE

Consequently, a possible configuration's devices for the 5L E-Type Inverter is shown in Fig. 4. The switches and diodes voltage rating are function of the maximum blocking voltage $V_{BL(max)}$ across the devices during the commutation. The blocking voltage $V_{BL(max)}$ at a steady state depends on the power devices position into 5L E-Type Inverter. The maximum blocking voltage across the switches S_{xyA} and S_{xyB} is V_{BUS}, whereas the steady state blocking voltage across the switches S_{xy21} and S_{xy22} is $½V_{BUS}$.

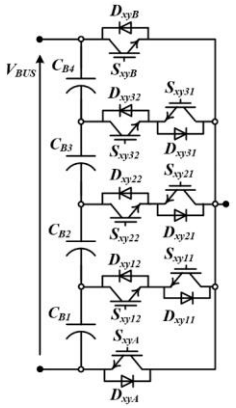


Fig. 4. Single leg 5L E-Type Inverter Configuration.

The blocking voltages of the switches arranged in the top-middle leg, S_{xy31} and S_{xy32}, are $¼V_{BUS}$ and $¾V_{BUS}$, respectively; moreover, the blocking voltages of the S_{xy11} and S_{xy12}, are $¾V_{BUS}$ and $¼V_{BUS}$, respectively. Besides the blocking voltage at steady state, the over-voltage commutation Δv that occurs during the commutation has to take into account. The over-voltage commutation Δv is defined as in (1), where k_R is the coefficient that takes into account the resonance of the DC-bus circuit, L_ξ is the commutation inductance, di_{sw}/dt is the device current slope and V_{FR} is the forward recovery voltage of the complementary freewheeling diode.

$$\Delta v = k_R L_\xi \frac{di_{sw}}{dt} + V_{FR} \tag{1}$$

Consequently, as shown in (2) the switches and diodes voltage rating are given by the sum of two terms: the maximum blocking voltage at steady state and the commutation over-voltage.

$$V_{sw} = \overbrace{V_{BL(\max)}}^{STEADY\ STATE} + \overbrace{k_R L_\xi \frac{di_{sw}}{dt} + V_{FR}}^{TRANSIENT} \tag{2}$$

The advantage of this topology is that each power device in the 5L E-Type Inverter are switched with the blocking voltage at a steady state equal to $¼V_{BUS}$. Consequently, the commutation over-voltage Δv only occurs with low blocking voltage at a steady state ($¼V_{BUS}$).

The total commutation inductance L_ξ is given by three parameters: inductance introduced by the PCB tracks that connects the switching devices to the DC-bus capacitor L_σ, the inductance related to the DC-bus capacitors ESL and finally, the inductance associated with the die and wire bond of the power semiconductors L_{SW}, (3).

$$L_\xi = L_\sigma + ESL + L_{SW} \tag{3}$$

If the current path involves more power devices, the commutation inductance and the conduction losses could have high values. The commutation path as well as the commutation inductance depend on the power converter topology and the modulation index. The worst-case scenario of the commutation inductance happens during the peak of the modulation index, as shown in Fig. 5a. Fig. 5a also illustrates the current path (blue and red line) in the 5L E-Type Inverter The commutation loop of the 5L I-Type Inverter is highlighted in orange. Assuming that the power devices and the antiparallel diodes have a certain package, the equivalent half-circuit diagram of the single-leg 5L E-Type Inverter is shown in Fig. 5b. During the peak of the

modulation index, the switch S_{xy32} is always "ON" and the switches S_{xy31}, S_{xyB} are controlled in opposite phase. In such condition, when S_{xy31} is "OFF" and S_{xyB} is "ON", the commutation inductance $L_{\xi,A}$ can be written as in (4). When the switch S_{xy31} is "ON" and the switch S_{xyB} is "OFF", the commutation inductance $L_{\xi,B}$ is given as in (5).

$$L_{\xi,A} = \overbrace{L_7 + L_8}^{L_{\sigma,A}} + \overbrace{ESL_3 + ESL_4}^{ESL_A} + \overbrace{L_{CB} + L_{EB}}^{L_{SW,A}} \quad (4)$$

$$L_{\xi,B} = \overbrace{L_4 + L_5 + L_6}^{L_{\sigma,B}} + \overbrace{ESL_3}^{ESL_B} + \overbrace{L_{C32} + L_{E32} + L_{C31} + L_{E31}}^{L_{SW,B}} \quad (5)$$

The worst commutation inductance strongly depends on the power devices placed on the PCB. Although the top-middle devices S_{xy31} and S_{xy32} are placed on the PCB close to the DC-bus capacitor and the AC-side, the inductance $L_{\sigma,B}$ is less than the inductance $L_{\sigma,A}$. The inductance related to the DC-bus capacitor ESL_A and ESL_B are small when compared to the others inductance, whereas the inductance L_{SW} depends on the manufacturing of the devices. When the power devices have the same package, the inductance $L_{SW,B}$ is twice $L_{SW,A}$. Assuming that the traces on the PCB are short, the value of the inductance $L_{\sigma,A}$ (or $L_{\sigma,B}$) is smaller than the inductance $L_{SW,A}$ (or $L_{SW,B}$). Hence, the commutation inductance $L_{\xi,B}$ is slightly greater than inductance $L_{\xi,A}$ due to the inductance of the package. Considering the IGBT H5 package, commutation inductance in the worst condition can be estimated close to 28 nH.

The 5L E-Type Inverter shows better conduction losses compared to the 5L I-Type Inverter. The 5L E-Type Inverter and the 5L I-Type Inverter operate with five voltage levels when the modulation depth M_0 has high values. In such condition, as it can be seen from Fig. 5a and Fig. 6, it easy to understand that the 5L E-Type Inverter shows a better commutation loop (highlighted in orange line) and the current path (blue and red line) compared with 5L NPC Inverter and 5L I-Type Inverter.

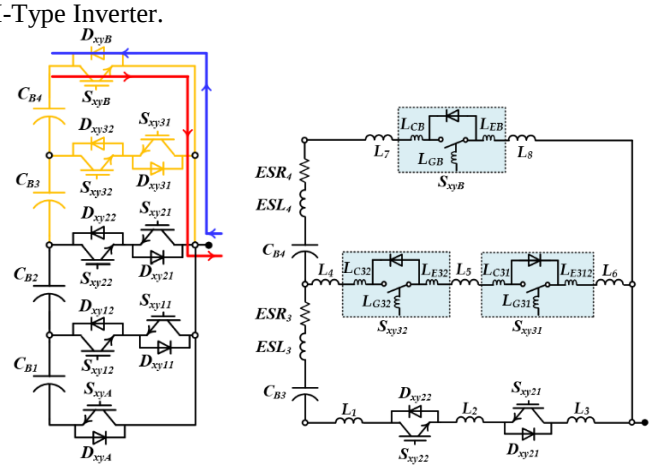


Fig. 5. Current paths for high modulation depth: (a) 5L E-Type Inverter, (b) Equivalent half-circuit diagram of the single-leg 5L E-Type Inverter.

In the 5L E-Type Inverter, the current flows through only one power device, S_{xyB} (or D_{xyB}), Fig. 5a. As depicted in Fig. 6, 5L I-Type Inverter's current path includes four power devices, T_{xy1}, T_{xy2}, T_{xy3}, T_{xy4}. The longer current path in the 5L I-Type Inverter causes higher over-voltage due to the high commutation inductance. Consequently, the voltage rating of the power semiconductors is increasing.

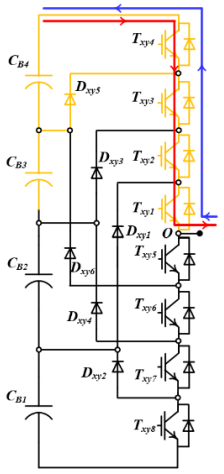


Fig. 6. Current paths for high modulation depth of the 5L NPC.

III. Interleaved 5L E-Type Inverter and Modulation

The interleaving is a form of paralleling technique where a single converter is replaced by N_C converters connected in parallel [20]. As it can be seen from Fig. 1, the number of the interleaved cells N_C is equal to 2. Using the interleaving topology each parallel converter is modulated by $2\pi/N_C$ shifted signal. By introducing a phase shift between the switching instants of the parallel converters of each phase, the amplitude of the total ripple current is reduced. Consequently, the harmonics content of the voltage improves due to the elimination of harmonics below $f_{sw}N_C$. If the current ripple is reduced and the voltage harmonics content improves, the interleaved topology allows to reduce the size of the required filter capacitance. Furthermore, sharing the current among the parallel converters, the interleaved converter enables the use of smaller lower current power devices than those used in a conventional converter. Thus, having the same power losses, it is possible to increase the switching frequency, allowing the reduction of the filter size.

The interleaved 3Φ5L E-Type Inverter modulation scheme is the well-known multilevel-PWM [20], which uses four different carriers per leg. In particular, the phase disposition carrier control technique has been selected for the proposed topology, as shown in Fig. 7. The carrier signals, c_{t11}, c_{t12}, c_{t13} and c_{t14} (solid line), are related to the leg 1 and the carrier signals c_{t21}, c_{t22}, c_{t23} and c_{t24}, in opposite phase (dashed line), are linked to the leg 2. All the carrier signals have the same amplitude and frequency.

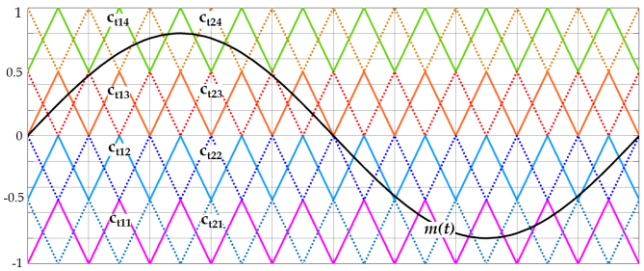


Fig. 7. Modulating scheme for the E-Type inverter.

For simplicity a pure sinusoidal modulating signal $m(t)=M_0 sin(\omega_0 t)$ is considered, where M_0 is the modulation depth and ω_0 is the output frequency.

Table 1. 5L E-Type Inverter Switching Conditions y∈{1, 2}.

	-1≤m(t)<-0.5	-0.5≤m(t)<0	0≤m(t)≤0.5	0.5<m(t)≤1
S_{xyA}	OFF if $m(t)>c_{ty1}(t)$ ON if $m(t)<c_{tv1}(t)$	OFF	OFF	OFF
S_{xy11}	ON	OFF if $m(t)>c_{ty2}(t)$ ON if $m(t)<c_{tv2}(t)$	OFF	OFF
S_{xy12}	ON if $m(t)>c_{ty1}(t)$ OFF if $m(t)<c_{tv1}(t)$	ON	ON	ON
S_{xy21}	ON	ON	ON if $c_{ty3}(t)>m(t)$ OFF if $c_{ty3}(t)<m(t)$	OFF
S_{xy22}	OFF	ON if $m(t)>c_{ty2}(t)$ OFF if $m(t)<c_{tv2}(t)$	ON	ON
S_{xy31}	ON	ON	ON	ON if $c_{ty4}(t)>m(t)$ OFF if $c_{ty4}(t)<m(t)$
S_{xy32}	OFF	OFF	OFF if $c_{ty3}(t)>m(t)$ ON if $c_{ty3}(t)<m(t)$	ON
S_{xyB}	OFF	OFF	OFF	OFF if $c_{ty4}(t)>m(t)$ ON if $c_{ty4}(t)<m(t)$

Each carrier controls two different power devices in opposite phase as: $S_{xyB} \leftrightarrow S_{xy31}$, $S_{xy32} \leftrightarrow S_{xy21}$, $S_{xy22} \leftrightarrow S_{xy11}$, $S_{xy12} \leftrightarrow S_{xyA}$. Table 1 illustrates the switches states according to the modulation index *m(t)*.

IV. Hardware Design Aspects

A. Resonant Balancing Circuit

As described in [7], [19], the SRBC is the variant of a switched capacitor converter. Fig. 8 shows the only bottom half side of the SRBC. A switch leg S_1, S_2 is connected across the capacitor C_{B1} and a switch leg S_3 S_4 is connected across the capacitor C_{B2}.

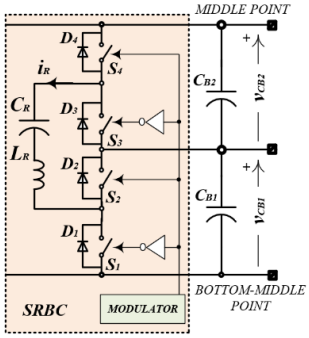


Fig. 8. Bottom half side Series Resonant Balancing Circuit (SRBC).

The capacitor C_R is the main switched capacitor that transfers the energy between the capacitors C_{B1} to C_{B2}. The inductor L_R is an auxiliary inductor used to reduce conduction losses and achieve zero current switching (ZCS) condition [21]. The switches S_1 to S_4 are driven with complementary control signals. The duty cycle d is constant, around 50%. The SRBC can be achieved using the series connection of four SK75GB066T modules, rated 60A-600V, where 4 µH and 16 µF are the values of the resonant tank. The prototype of the resonant balancing circuit is shown in [7], [8]. The SRBCs transfer power from the central capacitors (C_{B3} and C_{B2}) to the external capacitors (C_{B4} and C_{B1}) and vice versa, in order to keep the voltage distribution uniform among all the capacitors. However, the power distribution of the SRBCs is a function of the modulation depth M_0. Fig. 9 shows the Normalized partial power versus modulation depth.

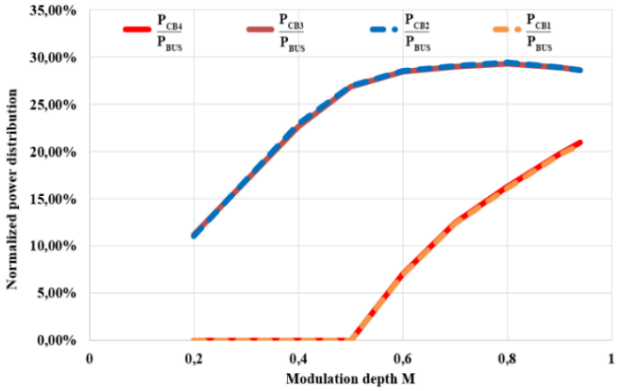


Fig. 9. Normalized partial power versus modulation depth M_0.

When the modulation depth M_0 is less than 0.5, the power is transferred from the inner capacitors (C_{B2}, C_{B3}) to the external capacitors (C_{B1}, C_{B4}). When modulation depth M_0 is above 0.5, the power passing through the external capacitors (C_{B1}, C_{B4}) increases. The maximum power transfer occurs when the modulation depth is close to 0.5. Since the 5L E-Type Inverter works with M_0 about equal 0.9, the power across the C_{B1}/C_{B4} reaches the rated value close to 20%, whereas the power through C_{B2}/C_{B3} is about 28% of the system power rating.

B. DC-bus Capacitors Selection

Assuming that the SRBCs reject the inverter current into DC-bus capacitors, as shown Fig. 10a, it is possible to achieve the condition (6).

$$i_{CB1} = i_{CB2} = i_{CB3} = i_{CB4} \tag{6}$$

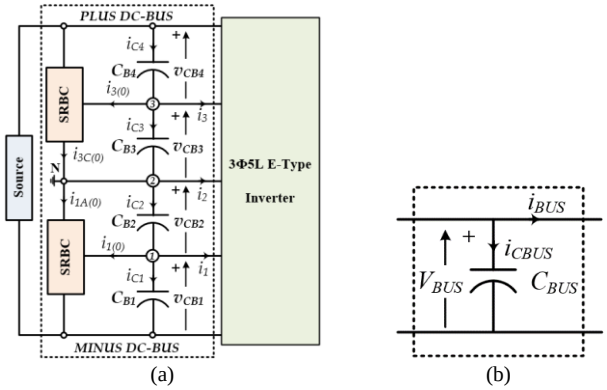
Consequently, an equal distribution between the series DC-bus capacitors (7) is obtained.

$$v_{CB1} = v_{CB2} = v_{CB3} = v_{CB4} \tag{7}$$

In such condition, the simplified circuit of the DC-bus capacitors is shown in Fig. 10. The low frequency current has strong impact on the capacitor losses, size, life time and cost. In order to optimize the system design (size and cost), low frequency current has to be reduced as much as possible. Considering that only the phase A is loaded and the current flow through the phase B and C is equal to zero (8), the low frequency capacitor instantaneous current is given by the equation (9), where V_0 is the RMS output voltage, I_0 is the RMS output current, ω_0 is the output frequency and φ_0 is the phase displacement between the output voltage and the corresponding output current at the fundamental frequency.

$$\begin{cases} i_A(t) = \sqrt{2} I_0 \sin\left(\omega_{OUT} t - \varphi_{OUT}\right) \\ i_B(t) = 0 \\ i_C(t) = 0 \end{cases} \tag{8}$$

$$i_{BUS,LF}(t)=\frac{V_0 I_0}{V_{BUS}}\left[\cos\varphi_0-\cos\left(2\omega_0 t\right)\right] \quad (9)$$



(a) (b)

Fig. 10. (a) Equivalent circuit diagram of the DC-bus capacitors; (b) Simplified circuit of the DC-bus capacitors.

Assuming that the SRBC compensates all the DC-bus current harmonics except 100 Hz component, the low frequency DC-bus capacitors current $i_{CBUS}(t)$ is given in (10).

$$i_{CBUS}(t)=\frac{V_0 I_0}{V_{BUS}}\cos\left(2\omega_0 t\right) \quad (10)$$

The RMS value of the double fundamental frequency is written in (11). Considering the scaling factor k as 1 at 100 Hz, the composite RMS current can be written as in (12).

$$I_{CBUS,(RMS)}\big|_{100Hz}=\frac{V_0 I_0}{\sqrt{2}V_{BUS}} \quad (11)$$

$$I_{CS,BUS(RMS)}=\sqrt{\left(\frac{I_{CBUS,(RMS)}\big|_{100Hz}}{k_{100Hz}}\right)^2} \quad (12)$$

Thus, the required minimum total DC-bus capacitor ($C_{BUS}=C_{B1}=C_{B2}=C_{B3}=C_{B4}$) can be obtained by the equation (13), where ΔV_{BUS} is the peak to peak voltage ripple, N_S is the number of series connected capacitors.

$$C_{BUS}=\frac{2\sqrt{2}}{\left(2\pi 100\right)\Delta V_{BUS}}N_S I_{CS,BUS(RMS)} \quad (13)$$

Considering P_0=20kW, V_0=230V, V_{BUS}=750V, ΔV_{BUS}=100V, and N_S=4, the minimum total capacitance value C_{BUS} is equal to 1100µF.

C. Inverter Devices Selection

The selection of the inverter devices has been done considering the voltage rating and stress current of the power semiconductors. Once the devices voltage ratings have been obtained, the selection of the device type and technology has been carried out. The use of 1200V IGBTs H3 have been found to be the best solution for the inverter outer switches S_{xyA}, S_{xyB}, D_{xyA} and D_{xyB} since they have to withstand the full DC-bus voltage. The 650V IGBT and Si-diode have been chosen for the power devices having $^1/_4V_{BUS}$, $^1/_2V_{BUS}$, $^3/_4V_{BUS}$ voltage ratings. In order to select the devices current rating, the average (AVG) and the RMS current flowing through the power semiconductors have been calculated. Considering V_0=230V, V_{BUS}=750V, M_0=0.87, T_j=100°C, number of interleaving cells N_c=2 and f_{sw}=24kHz, Table 2 shows the AVG and RMS current value for each power semiconductor as a function of the output power.

Table 2. RMS and Average numerical current of the Interleaved 3Φ5L E-Type Inverter x∈{A, B, C} and y∈{1, 2}.

		S_{xyA}, S_{xyB}	S_{xy11}, S_{xy12}, S_{xy31}, S_{xy32}	S_{xy21}, S_{xy22}
P_{out}=3kW	AVG [A]	0.49	0.43	0.05
	RMS [A]	1.19	0.95	0.2
P_{out}=5kW	AVG [A]	0.83	0.71	0.08
	RMS [A]	1.98	1.58	0.34
P_{out}=10kW	AVG [A]	1.67	1.43	0.16
	RMS [A]	3.95	3.19	0.68
P_{out}=15kW	AVG [A]	2.50	2.14	0.25
	RMS [A]	5.93	4.77	1.02
P_{out}=20kW	AVG [A]	3.34	2.86	0.33
	RMS [A]	7.91	6.36	1.36

The performance of the converter has been estimated considering two H3 series IGBTs rated 40A-1200V (S_{xyA}, S_{xyB}), two silicon freewheeling fast recovery diodes rated at 40A-1200V (D_{xA}, D_{xB}), six H5 high speed IGBTs rated at 50A-650V (S_{xy11}, S_{xy12}, S_{xy21}, S_{xy22}, S_{xy31}, S_{xy32}), six freewheeling rapid switching diodes rated 60A-650V (D_{xy11}, D_{xy12}, D_{xy21}, D_{xy22}, D_{xy31}, D_{xy32}) [12].

Table 3. 5L E-Type Inverter phase leg configuration, where x∈{A, B, C} and y∈{1, 2}.

Device	Part Number	Manufacturer	Technology
S_{xyA}, S_{xyB}, D_{xyA}, D_{xyB}	IKW40N120H3	Infineon	Si-IGBT H3
S_{xy11}, S_{xy12}, S_{xy21}, S_{xy22}, S_{xy31}, S_{xy32}	IGC16T65U8Q	Infineon	Si-IGBT H5
D_{xy11}, D_{xy12}, D_{xy21}, D_{xy22}, D_{xy31}, D_{xy32}	IDC08D65Q8	Infineon	Si-diode

Table 3 shows an overview of the components selection.

D. Output Filter Selection

The output inductor current is defined as in (14), where I_0 is the fundamental current and $\Delta i_{L0}(t)$ is high frequency current ripple.

$$i_{L0,x}(t)=\sqrt{2}I_0\sin\left(\omega_0 t\right)+\Delta i_{L0,x}\left(t\right) \quad (14)$$

Maximum peak-to-peak current ripple $\Delta i_{L,max}$ [20] is given in (15), where f_{sw} is the switching frequency.

$$\Delta i_{L,\max}=\left(\frac{V_{BUS}}{4}\right)\frac{1}{16 f_{sw}L_{0,x}} \quad (15)$$

Considering an ideal ICT and identical switching cells, the phase leg current can be written as in (16).

$$i_{01,x}\left(t\right)=i_{02,x}\left(t\right)=\frac{i_{L0,x}(t)}{2}=\frac{\sqrt{2}}{2}I_0\sin\left(\omega_0 t\right)+\frac{1}{2}\Delta i_{L0,x}\left(t\right) \quad (16)$$

The equivalent circuit diagram of the Interleaved 5L E-Type Inverter is depicted in Fig. 11, where $v_{0(sw),x}$ is the equivalent voltage source of two-cells inverter, $L_{0,x}$ is the output inductor and $C_{0,x}$ is the output capacitor.

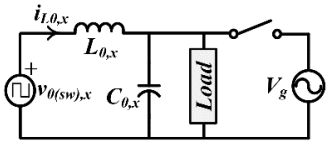


Fig. 11. Equivalent circuit diagram of the Interleaved 5L E-Type Inverter.

The selection of the inductance $L_{0,x}$ and capacitance $C_{0,x}$ is based on method explained in [20]. According to this analysis,

the output inductance and capacitor ($L_{0,x}$, $C_{0,x}$) are chosen equal to 80 µH and 6.8 µF, respectively.

V. Interleaved 5L E-Type Inverter Performance Results

The power losses of the converter have been derived in PLECS environment, which has a specific domain for modeling thermal structures and accurately calculates switching and conduction losses in power devices. This is accomplished through multi-dimensional lookup tables based on manufacturer information and experimental measurements. The conduction and switching losses are defined by look-up tables.

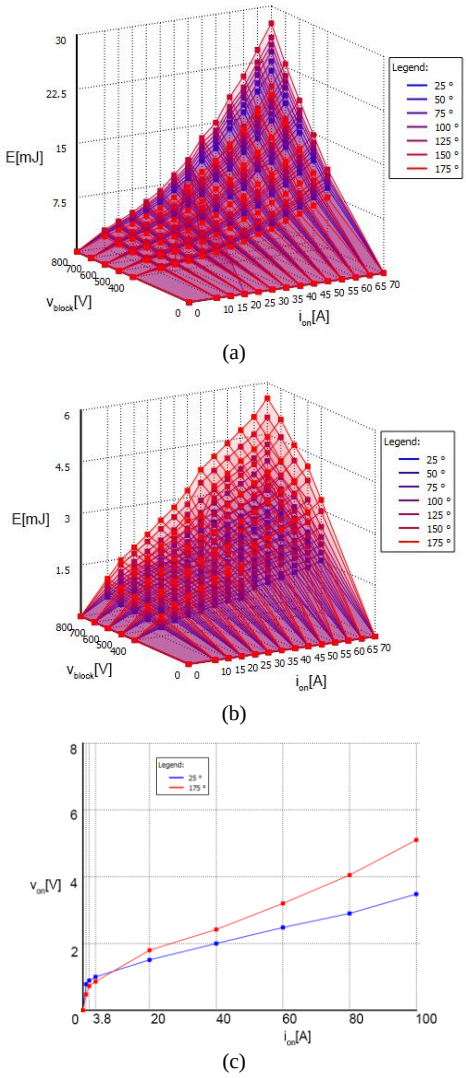


Fig. 12. Loss model of the IGBT IKW40N120H3. (a) Turn-on losses, (b) turn-off losses, (c) conduction loss model.

Using the data sheet of the power semiconductors listed in Table 3, the conduction and switching losses models have been built. Fig. 6 shows the example of the look-up tables linked to the conduction and switching losses of the power converter Si-IGBT H3.

PLECS shapes the switching losses as an energy pulse during switch commutation. The exact switching losses are calculated using the interpolation between the instantaneous values of the blocking voltage and the commutation current.

The performances of the Interleaved 3Φ5L E-Type Inverter including the SRBCs, DC-bus capacitors and output filter have been estimated considering the P_0=20kW, V_0=230V, V_{BUS}=750V, M_0=0.87, T_j=100°C, f_{sw}=24kHz and f_{swB}=20kHz (switching frequency of the SRBCs).

A. Performance of the 5L E-Type Inverter Devices

The losses and efficiency related to the power devices of the 3Φ5L E-Type Inverter are shown in Fig. 13. According to the nomenclature shown in Fig. 4, power losses versus output power related to the switches S_{xyB} (or S_{xyA}) are depicted in Fig. 14. The blue stacked column is linked to the conduction losses and the orange stacked column is related to the switching losses of the switches S_{xyB}.

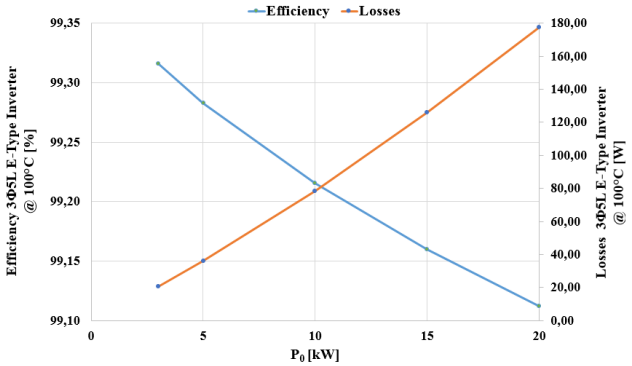


Fig. 13. Losses and efficiency of the 3Φ5L E-Type Inverter's devices versus output power.

It can be seen that the power losses of the switches S_{xyB} (or S_{xyA}) increase with output power.

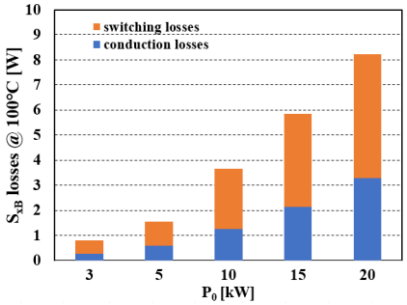


Fig. 14. Power losses of the outer IGBTs S_{xyB} (or S_{xyA}).

Fig. 15 shows both conduction and switching losses related to the power semiconductor located in top-middle (S_{xy32}, D_{xy31}) and bottom-middle (S_{xy11}, D_{xy12}) legs. On one hand, the IGBTs S_{xy32} (or S_{xy11}) shows a relatively high switching and conduction losses when the output power increases, Fig. 15a. On the other hand, the diodes D_{xy31} (or D_{xy12}) shows low switching losses, Fig. 15b. The power distribution linked to the power devices located in the middle-leg S_{xy21} and D_{xy22} (or S_{xy22} and D_{xy21}) are illustrated in Fig. 16. Their switching and conduction losses are strongly reduced due to low average conduction time and the number of commutations. Power losses distribution (conduction losses plus switching losses) related to each leg of the 3Φ5L E-Type Inverter versus output power is depicted in Fig. 17. It can be seen from Fig. 17 that the losses distributions exhibit an increasing trend when the output power increases and the outer legs (blue stacked) show higher losses compared to the other legs.

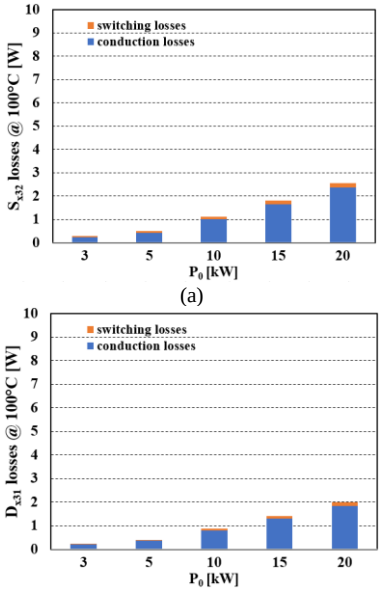


Fig. 15. Losses of the top-middle and bottom-middle legs versus output power: a) IGBTs S_{xy32} (or S_{xy11}), b) diodes D_{xy31} (or D_{xy12}).

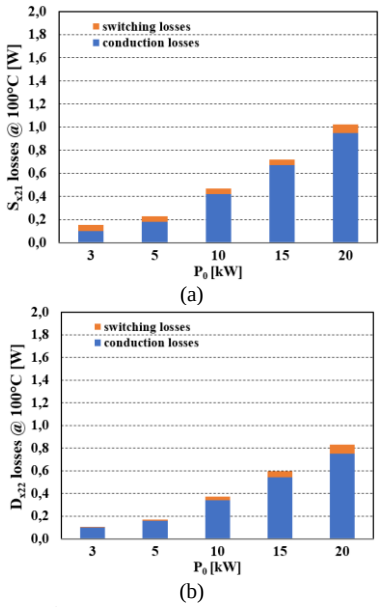


Fig. 16. Power losses of the middle leg: a) IGBTs S_{xy21} (or S_{xy22}), b) diodes D_{xy22} (or D_{xy21}).

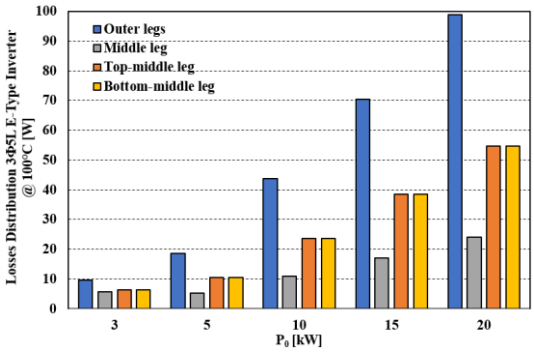


Fig. 17. Interleaved 3Φ5L E-Type Inverter losses distribution versus output power.

B. *Performance of the DC-bus Capacitors and SRBCs*

According to the previously analysis, selecting the capacitors EPCOS 390µF/400V with typical ESR of 130mΩ at 100Hz, the total losses of the DC-bus capacitors versus output power are shown in Fig. 18. Starting from the datasheet provided by the Semikron (Semitop3 SK75GB066T), Fig. 19 illustrates the estimated SRBCs losses versus output power.

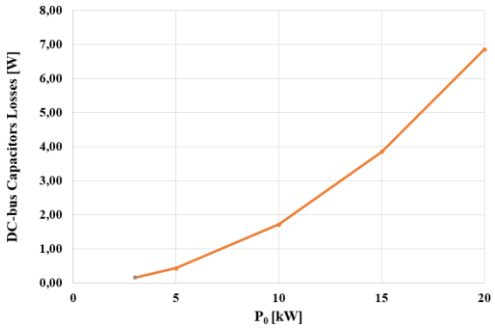


Fig. 18. Total DC-bus capacitors losses.

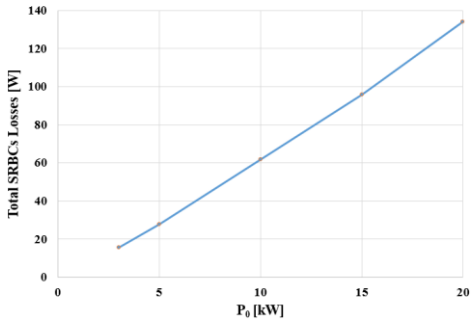


Fig. 19. SRBCs losses versus output power.

C. *Performance Output Filter*

According to the filter design shown in [20], the three-phase output filter losses as function of the output power are depicted in Fig. 20.

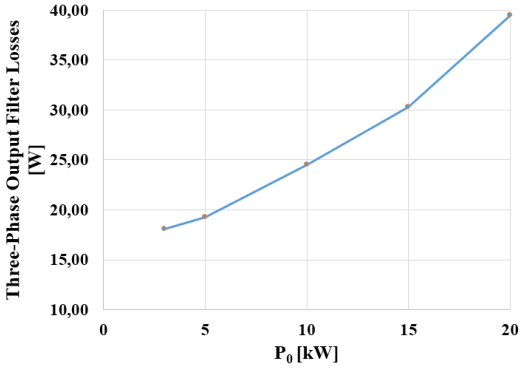


Fig. 20. Output filter losses versus output power.

D. *Total Performance of the Interleaved 3Φ5L E-Type Inverter*

Total losses and efficiency of the 3Φ5L E-Type Inverter's devices including the DC-bus capacitors, SRBCs and output filter are shown in Fig. 21. The green line is related to the efficiency, whereas the orange line is linked to the losses. It can be noticed the peak efficiency is about 98.34% and the nominal load efficiency is about 98.21%.

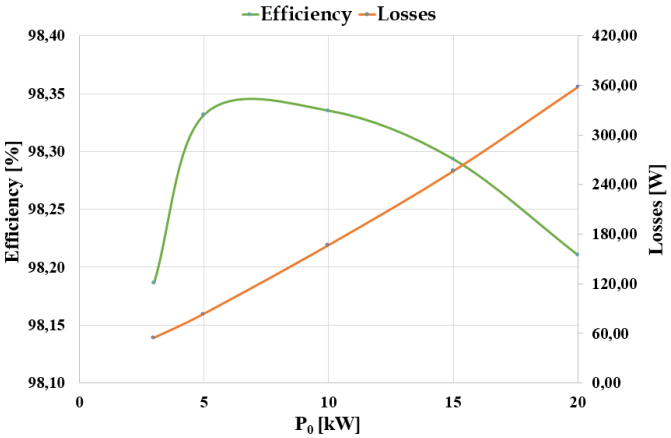


Fig. 21. Total losses and efficiency of the 3Φ5L E-Type Inverter versus output power.

According to the data-sheet bare dies of the IGBT H3, IGBT H5, Si-diode and the SK75GB066T modules, the total chip area of the SRBC normalized respect to the total chip area of the 3Φ5L E-Type Inverter is shown in Fig. 22. It can be noticed from Fig. 22, the chip area of the SRBCs is about 14.54% of the total chip area of the 3Φ5L E-Type inverter.

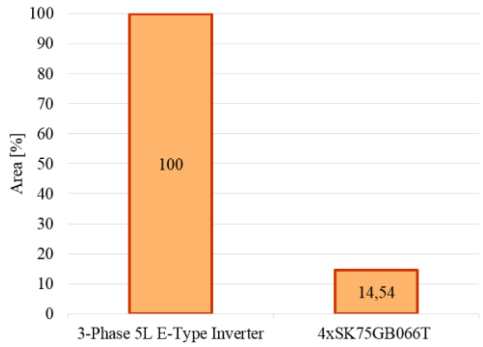


Fig. 22. Chip area of the SRBCs normalized respect to the area of the 3Φ5L E-Type inverter.

E. Discussion on Cost-Benefit Interleaved of the 3Φ5L E-Type Inverter

In this section a cost-benefit comparison between the Interleaved 5L E-Type Inverter and the Interleaved three level T-Type (3L T-Type Inverter) Inverter has been carried out. To better understand the huge benefits of the proposed inverter, figures of merit (FOM) such as cost, volume, power density, weight and specific power of the 3L T-Type Inverter and the 5L E-Type Inverter have been defined. Fig. 23 shows the FOM comparison between 3Φ5L E-Type Inverter and 3Φ3L T-Type Inverter normalized respect to the three-phase two-level Inverter. As it can be seen from Fig. 23, the 3Φ5L E-Type Inverter shows better volume, weight, power density and specific power compared to the 3Φ3L T-Type Inverter. On the other hand, the 3Φ5L E-Type Inverter exhibits a slight increment of cost. The cost comparison between the topologies has been carried out considering the price per unit.

The 3Φ5L E-Type Inverter uses 16 switches for each phase. The total chip area of the 3Φ5L E-Type Inverter is about 2290 mm^2. Whereas, only 8 switches per phase are used in the 3Φ3L T-Type topology, resulting in a total chip area of 1322 mm^2. On one hand, the amount of silicon for the 3Φ5L E-Type Inverter is larger than in the 3Φ3L T-Type Inverter. On the other hand, the amount of losses related to the 3Φ5L E-Type are lower than the 3Φ3L T-Type Inverter: 177 W and 300 W respectively. Thus, considering the same power semiconductor's technology, the losses related to the 3Φ5L E-Type Inverter power semiconductors are about 59 % of the losses in the 3Φ3L T-Type Inverter. Consequently, the heatsink size and weight for the 3Φ3L T-Type Inverter will be bigger than the on for the 3Φ 5L E-Type. With maximum heatsink temperature set at 80°C, the calculated heatsink volumes of the 3Φ5L E-Type Inverter and of the 3Φ3L T-Type Inverter are respectively 990 cm^3 and 1200 cm^3. Furthermore, the calculated total filter volume value of the 3Φ3L T-Type Inverter is 419 cm^3, whereas the total filter volume value for the 3Φ5L E-Type Inverter is 240 cm^3. As a result, more power devices are used in the 5L E-Type Inverter compared to the 3Φ3L T-Type Inverter with the benefit to reduce the size of the output filter and the heatsink.

The more stressed devices in the 3L T-Type Inverter and 5L E-Type Inverter are located in the external leg. The maximum voltage stress across the external devices of the 3L T-Type Inverter and 5L E-Type Inverter is the same (V_{BUS} =750 V).

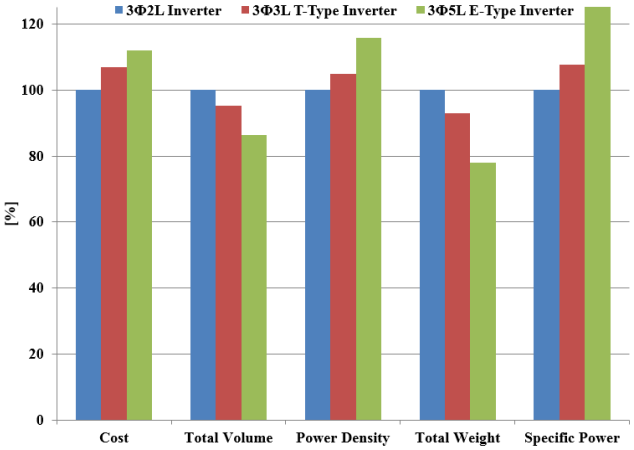


Fig. 23. FOM of the 3Φ5L E-Type Inverter and 3Φ3L T-Type Inverter normalized respect to the three-phase two-level Inverter. P_0=20kW, V_0=230V, V_{BUS}=750V, f_{sw}=24kHz.

In this condition, the commutation over-voltage Δv is zero in both inverters. However, all devices in the 5L E-Type Inverter are switched with the blocking voltage at a steady state equal to $¼V_{BUS}$. In the 3L T-Type Inverter all the devices are switched with the blocking voltage at a steady state equal to $^1/_2V_{BUS}$. Thus, in the 5L E-Type Inverter the commutation over-voltage Δv happens with a low blocking voltage. This means that the 5L E-Type Inverter shows better switching losses compared to the 3L T-Type Inverter. Additionally, keeping constant the device's losses, the 3L T-Type Inverter requires the increase of the switching frequency in order to achieve the same ripple in the output current. Thus, the output filter components in a 5L E-Type Inverter will be smaller in both value and size than the output filter components in a 3L T-Type Inverter (assuming the same switching frequency).

VI. Converter Control Strategy

The 3ΦN5L E-Type Inverter's control algorithm has been implemented using the LabVIEW development environment. The block scheme of the single phase 5L E-Type Inverter control strategy is depicted in Fig. 24. In the concurrent control two reference signals are tracking: output current and voltage

references ($i_{0,ref}$ and $v_{0,ref}$). The reference signals, $i_{0,ref}$ and $v_{0,ref}$, are defined in (17), where I^*_0 and V^*_0 are the output RMS current and voltage.

$$i_{0,ref}(t) = \sqrt{2} I_0^* \sin\left(\hat{\theta}_g\right), v_{0,ref}(t) = \sqrt{2} V_0^* \sin\left(\hat{\theta}_g\right) \quad (17)$$

The control always adjusts the output current during the "grid-tied operation mode". The control algorithm's operating mode changes in "islanding operation mode" when the grid fault occurs. The circulating current into ICT_0, $\Delta i_{L0}=i_{L0A}-i_{L0B}$, is controlled by an additional loop. The error signal, provided by the difference between $\Delta i_{L0,ref}=0$ and Δi_{L0}, is controlled by a proportional integral regulator. Thus, the ICT_0 circulating current can be adjusted by adding an offset into the modulating signals. As it can be seen from Fig. 24, the regulator of the concurrent control is the 3-Degree of freedom multi-resonant controller (MRC) [15]. The transfer function $G_{RC(n)}(s)$ is defined in (18), where n is the number of harmonics, $k_{ir(n)}$, $\theta_{(n)}$, $\omega_{cr(n)}$, and $\omega_{0(n)}$ are the gain, phase, width and resonance frequency of the controller, respectively; h is the maximum harmonic order that is included in the multi- resonant controller.

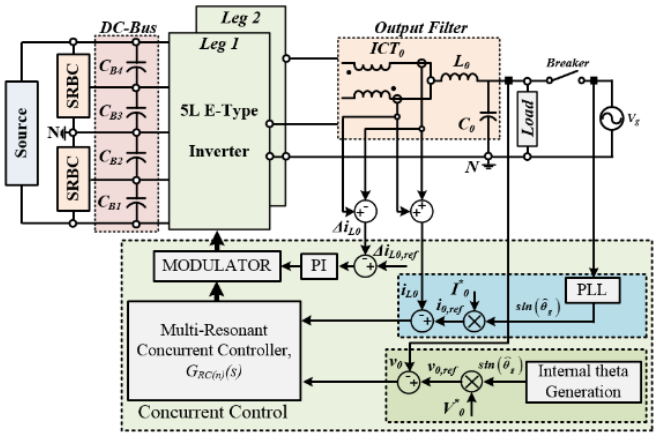


Fig. 24. Control loop structure Single-Phase 5L E-Type Inverter.

$$G_{RC(n)}(s) = \sum_{n=1}^{h} 2k_{ir(n)}\omega_{cr(n)} \frac{s\cos(\vartheta_{(n)}) + \omega_{cr(n)} - \omega_{0(n)}\sin(\vartheta_{(n)})}{s^2 + 2\omega_{cr(n)}s + \left(\omega_{cr(n)}^2 + \omega_{0(n)}^2\right)} \quad (18)$$

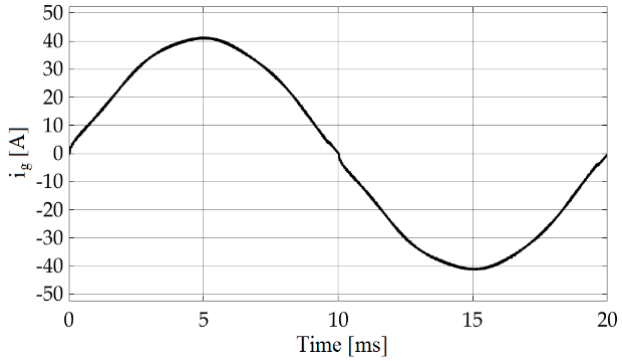


Fig. 25. Grid Current waveform i_g.

The single-phase phase-locked loop (PLL) system used to derive the grid phase $\hat{\theta}_g$ has been implemented according the method shows in [17].

When the inverter works in islanding operation mode, the grid angle is generated internally, see Fig. 24. The concurrent control has been implemented in LabVIEW environment according to the method shown in [22]. Fig. 25 shows the grid current i_g of the converter at nominal load.

VII. Experimental Results

Experimental tests have been performed on a 20 kVA inverter prototype in order to support the proposed analysis. The experimental results have been obtained using the local grid available in the laboratory. The DC-bus voltage has been properly provided by two series 400V/50A programmable DC power supplies. The proposed power conversion system is controlled by the National Instruments System-on-Module (sbRIO-9651) with a dedicated board specifically designed for power electronics and drives applications [22]. Fig. 26 illustrates the phase-to-neutral output switching voltages of the phase A $V_{sw,AN}$ and the DC-bus voltages V_{BUS}, considering the same operating conditions described in the section V.

As previously mentioned, the worst-case commutation path, which involves the devices located in the bottom-middle and top-middle legs, generates the worst-case over-voltage Δv. Fig. 27. shows the drain-to-source voltage $V_{S,A131}$ across the device S_{A131} and its current $I_{S,A131}$ at rated power during the turn-off. The current flow through the device is half of the output current due to the interleaving configuration.

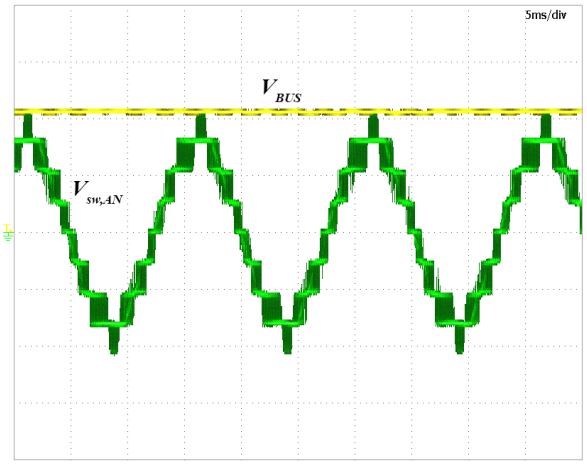


Fig. 26. Phase-to-neutral output switching voltages of the phase A, leg 1, $V_{sw,AN}$ and the DC-bus voltages V_{BUS}. Voltage 400 V/div.

As it can be seen from Fig. 27, the worst-case over-voltage commutation Δv is about 44 V.

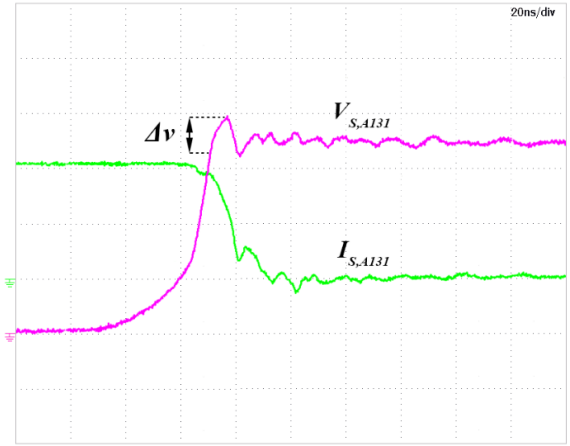


Fig. 27. Drain-source voltage and current related to devices S_{A131} during the turn-off. Voltage 50 V/div, Current 10 A/div.

Since the di_{sw}/dt is approximately equal to 2.1 A/ns, from equation (1) the commutation inductance is estimated to be 21 nH, which is slightly less than the estimated commutation inductance of 28 nH. Fig. 28 shows the phase-to-neutral output voltages V_{AN}, V_{BN} and the phase current I_{AN}, I_{BN}, in the case of resistive load. Total harmonic distortion of the output current THD_i, estimated considering the harmonic components up to the 50th order, is equal to 1.26 %. Thus, THD_i fulfils the international standards, such as IEEE STD 519-2014, EN 50160 and IEC 61000-2-4. Furthermore, the steady-state output voltage THD_v is about 0.7% for all of the three phase-to-neutral voltages. The experimentally achieved efficiency of the 3Φ5L E-Type Inverter is compared with the estimated efficiency in order to confirm the theoretical performance analysis, as shown in Fig. 29. It can be seen from Fig. 29 that the experimental results show a good matching compared to the theoretical analysis. Consequently, the achieved experimental points validate the theoretical performance analysis.

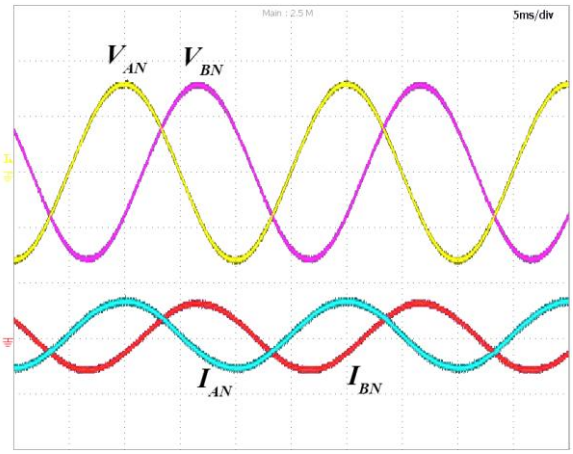


Fig. 28. Phase-to-neutral output voltages V_{AN}, V_{BN} and the phase current I_{AN}, I_{BN}. Voltage 200 V/div, Current 50 A/div

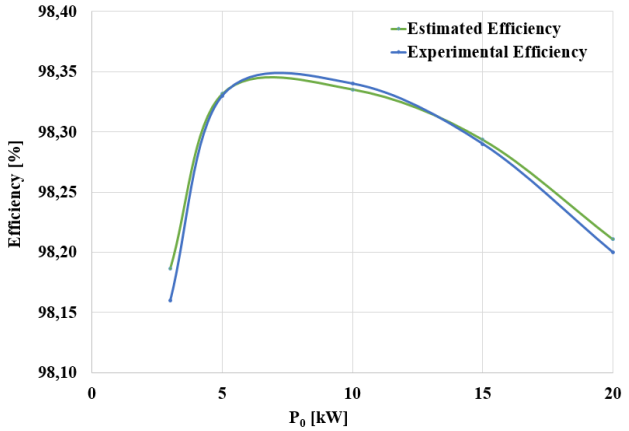


Fig. 29. Experimental and estimated performance of the 3Φ5L E-Type Inverter versus output power P_0.

CONCLUSIONS

The 3Φ5L E-Type Inverter for grid-connected applications has been presented and analyzed in this paper. The concept of the interleaving 3Φ5L E-Type Inverter using an ICT has been then explained and modulation strategy has been described. Converter's power losses distribution and design criteria have been presented. The proposed topology has been carefully studied by considering the combination of high speed IGBT and Si rapid switching diodes. The thermal model of power semiconductors has been created in PLECS environment, producing multi-dimensional lookup tables based on the parameters provided by the manufactures. The concurrent control strategy of the 3Φ5L E-Type Inverter has been described and implemented in LabVIEW environment. According to the analysis and design, an extraordinary peak efficiency of 98.34%, as well as THD_i of 1.26% and THD_v of 0.7% are achieved when the inverter works in grid-tied operation mode and islanding operation mode, respectively.

REFERENCES

[1] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg and S. Farhangi, "Optimal Selective Harmonic Mitigation Technique on Variable DC Link Cascaded H-Bridge Converter to Meet Power Quality Standards," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1107-1116, Sept. 2016.

[2] D. B. Vannoy, M. F. McGranaghan, S. M. Halpin, W. A. Moncrief and D. D. Sabin, "Roadmap for Power-Quality Standards Development," in IEEE Transactions on Industry Applications, vol. 43, no. 2, pp. 412-421, March-april 2007.

[3] A. Bindra, "APEC Signals Emerging Trends: A focus on advancements in GaN integration, SiC devices, high step-down converters, and passives," in IEEE Power Electronics Magazine, vol. 3, no. 2, pp. 57-62, June 2016.

[4] Z. Liu, B. Li, F. C. Lee and Q. Li, "High-Efficiency High-Density Critical Mode Rectifier/Inverter for WBG-Device-Based On-Board Charger," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 9114-9123, Nov. 2017.

[5] S. Rivera, B. Wu, R. Lizana, S. Kouro, M. Perez, and J. Rodriguez, "Modular multilevel converter for large-scale multistring photovoltaic energy conversion system," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 1941–1946.

[6] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, "Hybrid Cascaded Modular Multilevel Converter With DC Fault Ride-Through Capability for the HVDC Transmission System," IEEE Trans. Power Deliv., vol. 30, no. 4, pp. 1853–1862, Aug. 2015.

[7] P. Grbovic, A. Lidozzi, L. Solero, and F. Crescimbini, "Five-Level Unidirectional T-Rectifier for High-Speed Gen-Set Applications," IEEE Trans. Ind. Appl., vol. 52, no. 2, pp. 1642–1651, Mar. 2016.

[8] P. Grbovic, A. Lidozzi, L. Solero, and F. Crescimbini, "Performance evaluation for the five-level unidirectional T-rectifier in high-speed electric generating units," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015, pp. 5110–5116.

[9] S. A. Amamra, K. Meghriche, A. Cherifi and B. Francois, "Multilevel Inverter Topology for Renewable Energy Grid Integration," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8855-8866, Nov. 2017.

[10] P. J. Grbović, F. Crescimbini, A. Lidozzi, and L. Solero, "Multi-level converters for low voltage high current applications: Issues, challenges and limitations," in 2014 16th International Power Electronics and Motion Control Conference and Exposition, 2014, pp. 737–744.

[11] A. Hota, S. Jain and V. Agarwal, "A Modified T-Structured Three-Level Inverter Configuration Optimized With Respect to PWM Strategy Used for Common-Mode Voltage Elimination," in IEEE Transactions on Industry Applications, vol. 53, no. 5, pp. 4779-4787, Sept.-Oct. 2017.

[12] M. D. Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovic, "Five-level back to back E-Type converter for high speed gen-set applications," in IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, 2016, pp. 3409–3414.

[13] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Jul. 2004.

[14] A. Lidozzi, M. Di Benedetto, L. Solero, F. Crescimbini and P. J. Grbovic, "Fault tolerance analysis for the 5-level unidirectional T-Rectifier," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7.

[15] A. Lidozzi, M. Di Benedetto, S. Bifaretti, L. Solero and F. Crescimbini, "Resonant Controllers With Three Degrees of Freedom for AC Power Electronic Converters," in IEEE Transactions on Industry Applications, vol. 51, no. 6, pp. 4595-4604, Nov.-Dec. 2015.

[16] A. Esmaeilian and M. Kezunovic, "Prevention of Power Grid Blackouts Using Intentional Islanding Scheme," in IEEE Transactions on Industry Applications, vol. 53, no. 1, pp. 622-629, Jan.-Feb. 2017.
[17] S. Bifaretti, A. Lidozzi, L. Solero and F. Crescimbini, "Anti-Islanding Detector Based on a Robust PLL," in IEEE Transactions on Industry Applications, vol. 51, no. 1, pp. 398-405, Jan.-Feb. 2015.
[18] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti and F. Z. Peng, "Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation," in IEEE Transactions on Industrial Electronics, vol. 58, no. 1, pp. 147-157, Jan. 2011.
[19] K. Sano and H. Fujita, "Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters," IEEE Trans. Ind. Appl., vol. 44, no. 6, pp. 1768–1776, Nov. 2008.
[20] M. Di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini and P. J. Grbovic, "Analysis and design of LC filters for the 5-level 3-phase Back to Back E-Type Converter," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 3816-3821.
[21] J. Grbovic, P. Delarue, and P. L. Moigne, "A Novel Three-Phase Diode Boost Rectifier Using Hybrid Half-DC-Bus-Voltage Rated Boost Converter," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1316–1329, Apr. 2011.
[22] A. Lidozzi, M. Di Benedetto, V. Sabatini, L. Solero and F. Crescimbini, "Towards LabVIEW and system on module for power electronics and drives control applications," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 4995-5000.

Marco di Benedetto (S'16–M'18) received the M.Eng. degree in Electronic Engineering from the University of Roma TOR VERGATA, Rome (Italy), in 2014, and Ph.D. degree in Mechanical and Industrial Engineering from ROMA TRE University, in 2018.
Since November 2018, he is research fellow at Center of Power Electronics and Drives (C-PED) at the ROMA TRE University. His research interests are mainly focused on hardware and FPGA control design for multilevel power converter topologies for high speed generating and UPS applications.

Alessandro Lidozzi (S'06–M'08) received the Electronic Engineering degree and the Ph.D. degree from the Roma Tre University, Rome, Italy, in 2003 and 2007, respectively.
From 2010 to 2017, he was Researcher with the Department of Engineering, ROMA TRE University; where, since 2017, he has been Associate Professor. His research interests are mainly focused on power converter modeling and control, control of permanent magnet motor drives, control aspects for power electronics in diesel-electric generating units, four-leg converters and development of high-performance control platforms based on combined DSP-FPGA systems.

Luca Solero (M'98) received the Electrical Engineering degree from the University of Rome "La Sapienza," Italy, in 1994. Since 1996 he has been with the Department of Engineering, University ROMA TRE where he currently is a Full Professor in charge of teaching courses in the fields of Power Electronics and Industrial Electric Applications. His current research interests include power electronic applications to electric and hybrid vehicles as well to distributed power and renewable energy generating units. He has authored or coauthored more than 150 technical published papers. Since 2018, he serves as Vice-Chair the IEEE IAS Industrial Power Converter Committee IPCC. He serves as an Associate Editor of IEEE Transaction on Industry Applications. Prof. Solero is a member of the IEEE Industrial Electronics, IEEE Industry Applications, and IEEE Power Electronics Societies.

Fabio Crescimbini (M'90) received his degree in Electrical Engineering and the Ph.D. from the University of Rome "La Sapienza," Rome, Italy, in 1982 and 1987, respectively. From 1989 to 1998, he was with the Department of Electrical Engineering, University of Rome "La Sapienza," as the Director of the Electrical Machines and Drives Laboratory. In 1998, he joined the brand-new University named ROMA TRE, Rome, Italy, where he is currently a Full Professor of Power Electronics, Electrical Machines and Drives in the Department of Engineering. His research interests include newly conceived electrical machines and novel topologies of power electronic converters for emerging applications such as electric and hybrid vehicles and electric energy systems for distributed generation and storage.
Prof. Crescimbini served as a member of the Executive Board of the IEEE Industry Applications Society (IAS) from 2001 to 2004. In 2000, he served as Cochairman of the IEEE-IAS "World Conference on Industrial Applications of Electric Energy" and, in 2010, he served as Cochairman of the 2010 International Conference on Electrical Machines (ICEM). He was a recipient of awards from the IEEE-IAS Electric Machines Committee, including the Third Prize Paper in 2000 and the First Prize Paper in 2004.

Petar J. Grbović (M'05–SM'08) received the Dipl. Ing. (B. Sc.) and the Magister (M.Sc.) degrees from the School of Electrical Engineering, University of Belgrade, Serbia, in 1999 and 2005, and the Doctor (Ph.D) degree from the Laboratoire 'Électrotechnique et d'Électronique de Puissance de Lille, l'Ecole Centrale de Lille, France in 2010. In past 15 years, he has been with various international R&D centres (PDL Electronics-New Zealand, Schneider Electric-France, General Electric-Germany/USA & Huawei Technologies-Germany/China). Since 2016 he is a scientific member of Centre of Power Electronics and Drives, C-PED Lab., Roma TRE University, Italy. Recently he has been appointed as a Full Professor at the University of Innsbruck, Austria.
He published over 60 IEEE papers, 16 IEEE tutorials and a book "Ultra-capacitors in power Conversion Systems: Analysis, Modelling and Design in Theory and Practice". He has 17 patents granted and 9 patent applications pending.