LC Filter Design for On-grid and Off-grid Distributed Generating Units

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***Abstract*— The paper deals with the design procedure of an LC based output filter for three-phase inverters to be used in both off-grid and on-grid scenarios. The aim of this procedure is to provide guidelines and component selection criteria for reducing the inverter output switching ripple in order to limit the interaction with the control algorithm and to increase the filter stability. A suitable combination of resistive and reactive components is used to realize the complete filter structure. The proposed procedure is applied to the design of the output power filter for a 40 kVA three-phase inverter.**

I. INTRODUCTION

Distributed generation is being developed worldwide to meet the increasing energy demand as well to reduce the environmental impact of fossil-fuel based centralized generation. Conventional electric power plants have rated power of thousands MVA and are usually located far from the load areas where the energy supply is needed. On the contrary, distributed generation systems are accomplished by using renewable energy generating units (e.g., photovoltaic arrays and wind turbines) which have relatively low power rating and are suitably connected to the power grid at the voltage level of the electricity distribution network so that the significant investment in electric transmission infrastructure can be substantially reduced. However, due to the intermittent nature of the renewable energy sources and the desire for generating operation with maximum power point tracking, an energy storage is usually needed and thereby the various electric power sources are operated in parallel against a common DC link by means of power electronic converters, as schematically shown in Fig. 1. Hence, a DC-AC converter with 4-wire output is used for connecting the generating system to the distribution network and the user loads, being such a converter required to provide both active and reactive power output depending on whether it is operated on-grid or off-grid. In this scenario, the electricity users can rely on self-produced energy from renewable sources to supply their own loads, whereas the power being in excess can be sold to the grid operator whenever even the local energy storage is fully charged. In case of short supply of energy, from both the renewable sources and the energy storage, the supply of the electrical loads is accomplished through the distribution network. On the other hand, if the grid fails, the generating system is disconnected from utility grid and the DC-AC converter is required to provide the electrical supply for the local loads.

In consideration of the modes of operation being envisaged for the DC-AC converter, the harmonic spectrum of the converter output voltage must be carefully considered in terms of harmonic content. It is possible to divide the spectrum of the converter output voltage into two main portions, i.e. the one related to fundamental frequency harmonics (low frequencies) and the one that concerns the switching harmonics (high frequencies). The first portion contains what the converter has to supply to the load, e.g. the 50Hz component in a standard grid-tied inverter. The second portion contains a set of undesired frequencies that are related to the converter switching behavior. As it is well known, a filter is needed for removing or, at least, for reducing the high-frequency content in the output voltage waveforms, thereby allowing only the low frequencies to pass through. To date, among the various filter configurations that have been proposed in the literature to the goal of reducing the harmonic content due to the converter switching, the most widely used schemes are based on the LC and the LCL filters topologies.

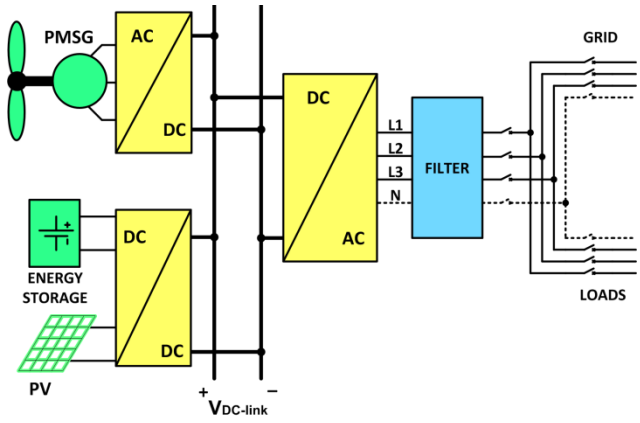

Figure 1. Distributed generating unit for on-grid and off-grid applications.

The LCL filter type is recommended in particular for grid-tied applications, since the presence of the second inductor makes the filter response more immune to grid parameters variation. This configuration makes it possible to obtain an output current ripple extremely reduced using inductors of relatively small value, compared to those of LC configuration with similar performances [1-2]. However, the excessive reduction of the inverter side inductor would significantly increases the current ripple flowing through the

power electronic devices. Switching and conduction power losses in inverter are also related to output current ripple content; thus, efficiency can be reduced especially at low power operating conditions.

The filter configuration derived from the LCL circuit and named as LLCL has been proposed in recent literature [3]. In this configuration, the LCL capacitor is replaced by an LC series circuit, tuned to resonate at the switching frequency. The presence of the LC circuit is intended to provide a near-zero impedance path for the residual switching component flowing through the main inductor. This feature allows to strongly reduce the output switching component when compared to the conventional LCL filter with same component values. However, it causes the reduction of the filter roll-off due to the high impedance of the LC series circuit at high frequency. In addition, in the LCL and LLCL filter, the inductor on the inverter side and the one on the grid side have to carry the full line current; even if the inductances value is quite reduced with respect to LC filter topology, the resulting cost and size are still important.

An alternative to the previously described configuration is the LC filter equipped with a tuned trap filter section [4]. The tuned trap-filter [5-6] has the LC-series configuration and is tuned at the output current ripple fundamental frequency. This filter is intended to reduce the output voltage switching ripple by giving a quasi-zero impedance path for the residual switching component flowing through the main inductor. In this way, similar performance of the LLCL filter can be achieved; however, only one line current sized inductor is used.

Both LC-based and LCL-based filter topologies present resonance phenomena at their characteristic frequency. The resonance can be suitably damped through a proper resistor, to be placed either in parallel or in series with the inductor or the capacitor. Conventional schemes show this resistor in series with the capacitor [7-10]. However, when the resistor is selected to obtain similar behavior of the Butterworth type second order low-pass filter, the LC roll-off at high frequency changes from -40 dB/dec to nearly -20 dB/dec. This drawback can be avoided by using a properly tuned series RLC circuit, placed in parallel connection with the LC capacitor, in order to selectively damp the LC characteristic resonance. In fact, with respect to its resonance frequency, the series RLC circuit shows high impedance at low and high frequencies and impedance equal to R at its resonance. As a consequence, it is possible to make the damping resistor visible only for a reduced frequency range, without degrading the low impedance at high frequency of the capacitor of the main LC filter and assuring, at the same time, satisfactory damping for the LC filter.

Active damping of the natural LC resonance has been investigated in recent literature [11, 12]. The virtual resistor technique acts on the control algorithm parameters in order to adjust the converter internal impedance. However, additional current sensors are required to perform this task; as well control platform advanced performances are essential to correctly operate at the LC resonance frequency.

This paper deals with the design procedure of an LC output filter, with either single or multiple tuned trap-filters. Suitable damping is achieved by means of a properly sized damping circuit. Each element added to the basic LC filter is designed to accomplish a specific task in order to shape the desired whole filter frequency response.

II. PROPOSED FILTER ARCHITECTURE

Proposed filter architecture is intended to be used in application for either grid connected or off-grid operations. As a consequence, local loads can be supplied through both the grid and the distributed generating units. When single-phase loads have to be supplied during off-grid mode of operation, a four wires inverter (either 4-legs or split dc-link) is required. Complete phase-to-neutral scheme of the investigated output filter is shown in Fig. 2, where the LC_{main} section of the filter is a standard second order passive low-pass filter, composed by a power inductor and a high current ripple film capacitor. This basic topology is combined with one or more either LC or RLC tuned circuits, placed in parallel with the main capacitor C_F.

In conventional LC filter, main inductance and capacitance p.u. values are quite high. Such values are usually found because of the required attenuation to eliminate the switching components and, at the same time, for satisfying the desired roll-off. Such design criteria exhibit the drawback of significant reactive current, which does not depend on load conditions. This results in oversizing of the filter main capacitors that have to be able to manage the flowing current. In the proposed filter structure, main capacitor has been strongly reduced with respect to conventional LC filter [12], improving the filter impedance at the fundamental frequency and dramatically reducing the reactive current component.

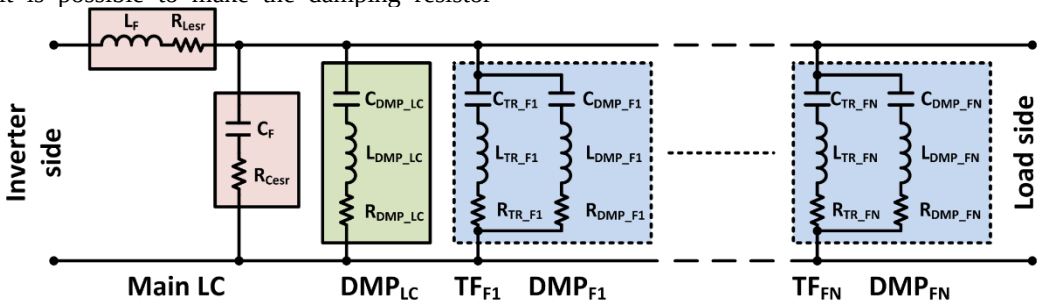

Figure 2. Proposed topology for the inverter output power filter.

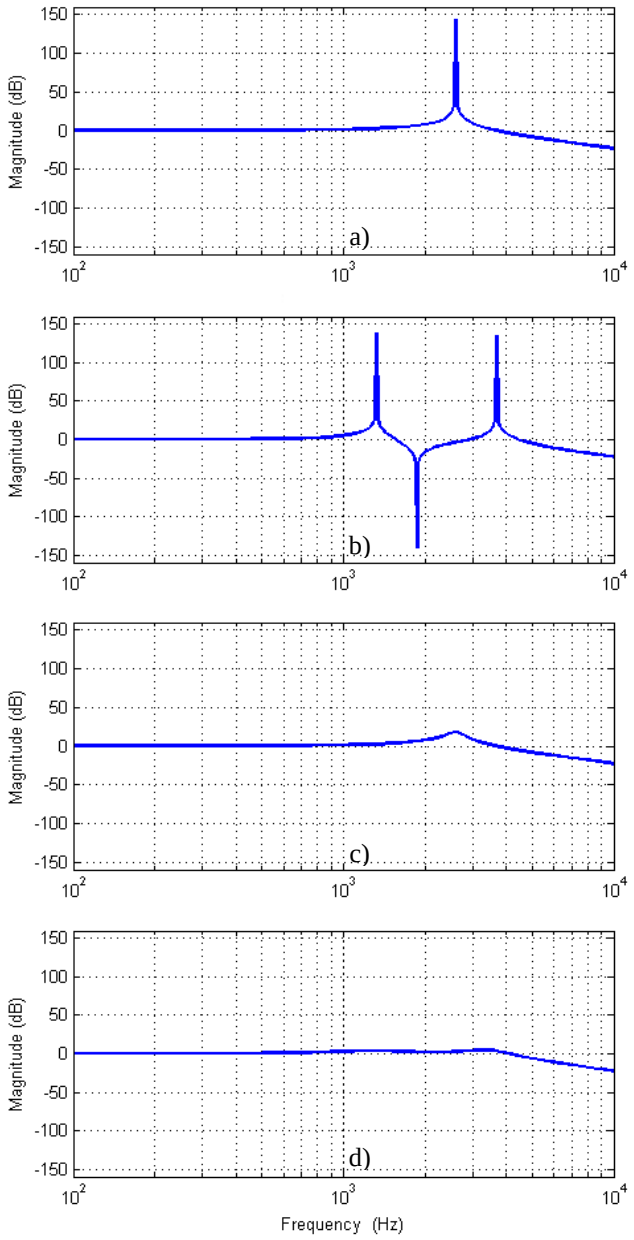

Figure 3. Transfer function of: a) LC_{main} , b) LC_{main} + DMP_{LC} with R_{DAMP_LC}=0Ω, c) LC_{main} + DMP_{LC} with R_{DAMP_LC}=100Ω, d) LC_{main} + DMP_{LC} with R_{DAMP_LC}=15Ω.

The natural resonance of the LC_{main} section, shown in Fig. 3a, is damped by the DMP_{LC} leg. The interaction between the DMP_{LC} and LC_{main} produces a double resonance phenomenon, as depicted in Fig. 3b; for this reason, DMP_{LC} circuit is tuned in order to properly damp the originated double resonance. R_{Lesr}, R_{Cesr}, $R_{TR\_F1\text{-}FN}$ are the equivalent series resistances of respectively main inductor, main capacitor and trap filters. Whereas, $R_{DMP\_LC,\ F1\text{-}FN}$ are the physical resistors of damping circuits. The presence of the damping circuit is highly suggested in the proposed reference application. In fact, in standard grid-tied inverter, resonance is not a so critical issue, provided the LC parameters are chosen in order to place the resonance far from system critical values (i.e. the maximum control bandwidth frequency and the switching frequency). However, dealing with local loads, especially when operating in off-grid mode, may lead to unpredictable results due to their unknown nature (linear, nonlinear, switching, etc.). For this reason, it is safer that output filter presents no resonance points at no load condition or, at least, that the resonance is properly damped.

The R_{DMP_LC} resistor value is critical for the correct operation of the DMP_{LC} circuit. In fact, choosing a low R_{DMP_LC} resistor value would lead to the effect depicted in Fig. 3b, where the DMP_{LC} circuit interacts with the LC_{main} circuit producing a double resonance. On the other hand, a too high resistance value would lead to only partial resonance damping as shown in Fig. 3c. The proper choice of R_{DMP_LC} resistor value allows to correctly damp the LC_{main} resonance, as depicted in Fig. 3d. The main benefit of the proposed damping circuit is the negligible influence on the LC_{main} roll-off at high frequency. The complete behavior at no load is highlighted in Fig. 4, where the effect of the conventional LC damping scheme, based on the positioning of the damping resistor in series with the LC capacitor, is compared with the proposed selective damping scheme. The analysis is carried out at no load condition, which is the most critical concerning the filter behavior at the resonance. Filter performance at loads with different power factor values are afterwards verified, as well they are taken into account for the power electronic converter controllers' design [13]

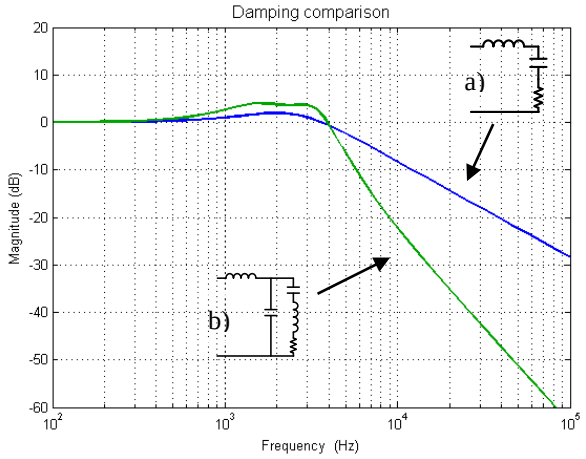

Figure 4. No load transfer function of: a) LC_main section with conventional damping scheme (R_damp=15Ω), b) LC_main section with proposed damping scheme (R_damp=15Ω).

The trap filters TF_{F1} through TF_{FN} are LC tuned circuits; in this case, their task is to provide a negligible impedance path for a limited set of frequencies around the switching frequency and its multiples. The range of frequencies, for which a trap filter shows negligible impedance, depends on the respective LC inductance and capacitance values. In fact, for a desired tuned frequency there are infinite combinations that lead to the same resonance frequency. However, these combinations differ for the shape of the impedance transfer function (TF). As an example, the behavior of the 12 kHz

tuned trap filter is depicted in Fig. 5, for different combinations of L and C values. In the proposed application, the trap filters are used to significantly reduce output switching harmonic components.

As it is known from the literature, the output voltage spectrum of a PWM inverter presents switching components not only at the switching frequency and respective multiples, but also in the neighborhood of these frequencies in the form of sidebands. Therefore, the shape of impedance transfer function of the trap filter needs to be sufficiently wide to present a negligible impedance value even at the sideband switching frequencies. Moreover, due to their undamped behavior, trap filters produce resonances when combined with the other elements of the filter circuit, as it is shown in Fig. 6 where the 12 kHz tuned trap filter is in cascade connection with the conventional LC filter.

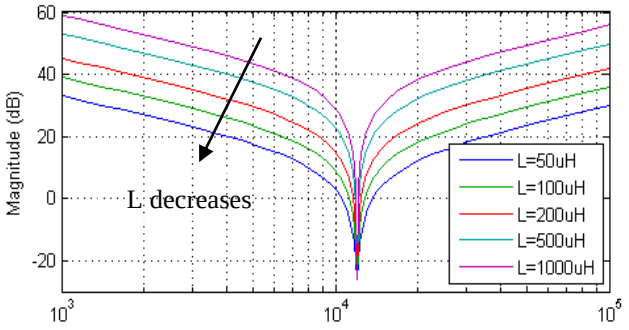

Figure 5. 12 kHz tuned trap filter impedance Bode diagram with different inductance and capacitance values.

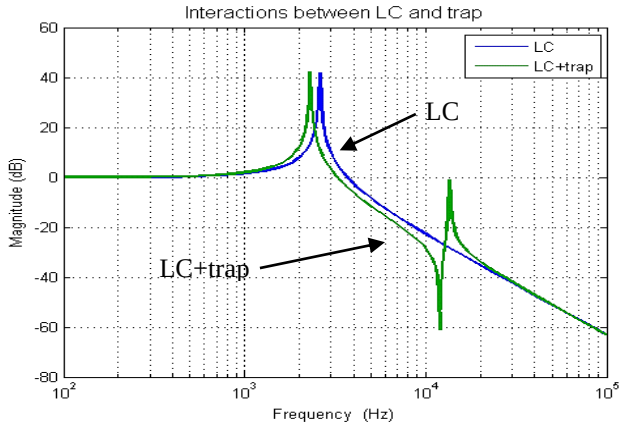

Figure 6. LC transfer function without (blue trace) and with (green trace) trap filter.

Appendix A describes the analytic calculation for this type of configuration. This behavior is similar to the one already depicted for the DMP_{LC} circuit (Fig. 3b); however it is not possible to increase the trap filter resistor value, because of the previously mentioned required low impedance, in order to provide improvements in attenuation of switching related sidebands with respect to the standard LC filter. For this reason, each trap filter is equipped with its own RLC damper circuit (DMP_{F1} and DMP_{F2}), properly sized to reduce resonance effect. It is to be noted that, changing from off-grid to grid-tied mode, the filter transfer function is modified in both shape and type as the control output moves from current to voltage regulation. In particular, shape is affected by grid impedance; in fact, in weak grids, the presence of grid impedance, which is considered purely inductive, leads to an LCL-type equivalent filter circuit, whose resonance frequency is different from the initial LC_{main} resonance frequency. Thus, the above described DMP_{LC} circuit can be ineffective. This is not, however, a concern; since in grid-tied mode disturbances caused by loads are mainly absorbed by the grid and the filter shape does not present significant amplifying resonances. For these reasons, the proposed design procedure is referred to the off-grid mode of operation.

III. Filter Components Design Criteria

In this section, general criteria for complete filter components sizing are given with reference to the scheme shown in Fig. 2. LC_{main} inductor is chosen on the basis of maximum allowed current ripple in the inverter switching devices. Moreover, its reactance should be less than 10% of system base impedance, in order to limit reactive voltage drop and required DC-link voltage value [1].

Maximum value for the LC_{main} capacitor is chosen starting from the acceptable power factor (PF) reduction at rated power. In fact, PF reduction depends on both LC_{main} capacitor value and on the capacitors values of the other tuned RLC circuits, as they present a nearly totally capacitive behavior at low frequency (i.e. at fundamental frequency). Thus, a good starting point is to calculate the maximum total capacitance for a given PF reduction (C_{max_PF}), and reserve approximately 30% of this capacitance to the LC_{main} capacitor, C_F of Fig. 2. This low percentage is due to the fact that one of the other capacitive elements of the circuit (C_{DAMP_LC}) may have a larger value than C_F, as will be explained later in the text. Thus, adequate margin should be taken into account for C_F value in order to properly size the complete filter.

The LC_{main} capacitance minimum value is set on the basis of considerations on the output voltage ripple value, with the aim to reduce first harmonic switching component and, consequently, also the higher order components. As a result of the target application requirements, minimum value can be larger than the previously selected C_F value. In this case, it is mandatory to place a trap filter tuned at the switching frequency, and shift the voltage ripple constrain to the next switching harmonic. This step can be iterated placing additional trap filters, until the resulting minimum capacitance value is consistent with the previously selected C_F.

DMP_{LC} circuit components are chosen in order to obtain a tuned frequency between 0.7 and 0.8 times the LC_{main} resonance frequency. Assuming L_{DMP_LC} value of the same order of magnitude of L_F, C_{DMP_LC} results 1.4-1.6 times C_F, i.e. in the order of 45-50% of C_{max_PF}. Due to the complex interactions between the tuned circuits in the filter, the

DMP_{LC} leg values cannot be achieved by simple closed form expressions; hence, they are achieved using a numerical trial-and-error iterative approach. An example of the above mentioned interactions can be noticed in Fig. 6, where the addition of the trap filter moves the LC_{main} resonance at lower frequency values.

Trap filters components' values have to be selected starting from the analysis of the output voltage spectrum of the PWM inverter, identifying the sidebands to take into account and how much they need to be reduced. Results of this procedure depend on system parameters as, for example, DC-link voltage, inverter output voltage, modulation index, modulation type, ratio between switching frequency and fundamental frequency, etc…

In trap filters capacitor sizing, trap-filters and dumpers related capacitance should be limited to the remaining 20-25% of the previously introduced C_{max_PF}. Small capacitors in parallel configuration are to be preferred, in order to reduce the effect of components' tolerances as well to obtain a wider range of possible values. On the other hand, trap filter inductor has to be chosen paying attention to the core A_L [nH/n.turns^2] value and its performance with respect to the product Ampere × number of turns. In fact, if the A_L value is not nearly constant up to the expected maximum current value, inductance value would change and dynamically de-tune the trap filter reducing its effectiveness. A nearly constant A_L values can be obtained by choosing inductor cores with almost constant permeability versus current, e.g. *sendust* (85% iron, 9% silicon and 6% aluminum) or *high-flux* (50% nickel and 50% iron).

Damper circuits for trap filters do not require particular care for the choice of components tolerance, due to their less selective behavior with respect to trap filters. With reference to the positive resonance of the trap filter, as it is shown in Fig. 6, inductors and capacitors are chosen in order to obtain a resonance frequency in the range 1.05-1.20 times the trap filter resonance, while optimal damping resistor is to be found by means of either simulation or trial and error procedure.

IV. Filter Design Example

In this section, the complete proposed procedure for filter design is applied to a 40 kVA 4-wire 4-leg inverter, with 680 V DC-link, 230 V_{rms} output phase voltage, 50 Hz fundamental frequency and 12 kHz switching frequency. A LabView code has been developed to assist the designer during the design process. In this example, components' values are expressed in both p.u. and absolute values. Calculations of the output voltage spectrum for residual ripple estimation are performed using the expression (1) for the Symmetrical Regular Sampled PWM, as illustrated in [14],

$$v_{out}(t) = \frac{4 \cdot V_{DC}}{\pi} \sum_{\substack{m=0 \leftrightarrow n=1 \\ m>0 \leftrightarrow n=\infty}}^{\infty} \sum^{\infty} \frac{1}{q} \cdot J_n\left(q \cdot \frac{\pi}{2} \cdot M\right) \cdot \sin\left(\left[q+n\right] \cdot \frac{\pi}{2}\right) \cdot \cos\left(m\left[\omega_{fsw} t + \theta_{fsw}\right] + n\left[\omega_{fund} t + \theta_{fund}\right]\right) \quad (1)$$

with

$$q = m + n\left(\omega_{fund} / \omega_{fsw}\right) \quad (2)$$

A. Step 1, LC_{main} components values

Inductors are chosen on the basis of the current ripple peak-to-peak value of 10% of the rated current. The achieved value for these components is 0.059 p.u. (i.e. 750 µH) of the base inductance, and complies with the previously shown 10% base impedance limit at 50 Hz.

Maximum total capacitance value is calculated on 0.02% power factor reduction at rated power, which corresponds to 2% of reactive power at full load and 4% of reactive power at half. This value allows maintaining a low power factor reduction even in the case of light load. In particular, when light resistive load are used, a small capacitor value grants a better efficiency, being the current mostly carried by IGBTs rather than diodes. Moreover, with this limit the no-load current is only 2% of the rated current, producing negligible incremental losses in both active and passive components. The calculated C_{max_PF} value is 0.02 p.u. (i.e. 16 µF), so C_F=0.0062 p.u., corresponding to 5 µF, is chosen as LC_{main} capacitor. Minimum LC capacitor value is calculated on the basis of the 1% of voltage ripple amplitude limit with respect to the phase voltage peak value. Calculated minimum C_F value is 0.129 p.u., equivalent to 103.5 µF, that is not consistent with maximum allowable value. Thus, the trap filter at switching frequency is to be added to the filter and the minimum value is now calculated on the basis of the desired voltage ripple value with reference to switching harmonics starting from $2m_f$ sidebands, where the frequency modulation ratio m_f is equal to the ratio between switching frequency and fundamental frequency. Calculated value is 0.0123 p.u. (9.9 µF); hence, a second trap filter is to be added. Iterating this procedure with reference to switching harmonics starting from $3m_f$ sidebands, with the same voltage ripple constrain of 1%, the minimum value of 0.003 p.u. (2.38 µF) is found, meaning that LC_{main} section design is complete with the results shown in Fig.7.

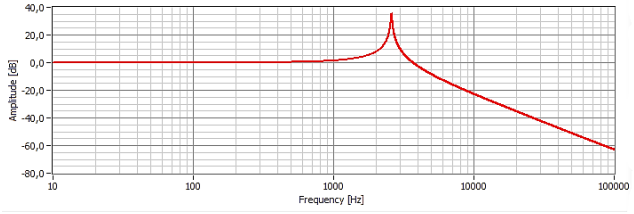

Figure 7. LC_{main} design results.

B. *Step 2, the DMP_{LC} circuit*

Based on both the LC_{main} selected values and the previously described criteria, the resonance frequency of approx. 2 kHz is chosen for the DMP_{LC} circuit. In order to limit the inductance value and inductor overall dimensions, C_{DMP_LC}=0.009 p.u., (7.2 µF), capacitor is chosen. Consequently the L_{DMP_LC}=0.064 p.u., (810 µH), inductor is chosen. The proper damping resistor for this configuration is found to be around R_{DMP_LC}=5.34 p.u., (21 Ω). This value is calculated considering the RLC DMP_{LC} circuit and solving it for the damping factor ζ=1 (i.e. behavior similar to Butterworth type second order low-pass filter).

$$\varsigma = \frac{R_{DMP\_LC}}{2}\cdot\sqrt{\frac{C_{DMP\_LC}}{L_{DMP\_LC}}} = 1 \rightarrow R_{DMP\_LC} = 2\cdot\sqrt{\frac{L_{DMP\_LC}}{C_{DMP\_LC}}} \quad (3)$$

It is to be noted that this value is only a suggestion and do not perform the complete damping of the LC resonance. The complete damping is in fact impossible, due to the double resonance introduced by the interaction between the LC_{main} and the DMP_{LC} circuits, as previously depicted in Fig. 3b. Tolerances in the DMP_{LC} components values are found to not produce appreciable variation in the DMP_{LC} circuit performances. Results for this design step, implemented through a suitable Labview code, are shown in Fig.8.

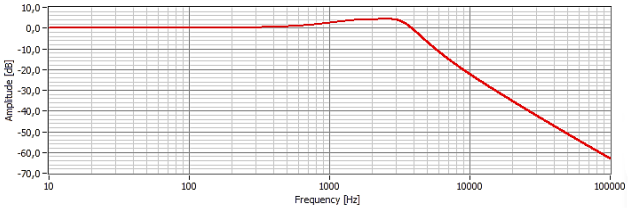

Figure 8. LC_{main} + DMP_{LC} circuit design results.

C. *Step 3, trap filters*

Based on step 1 results, two trap filters are needed for the target application filter. The first is centered at the switching frequency of 12 kHz and the second at 24 kHz. For both trap filters, the capacitor value of C_{TR_F1}= C_{TR_F2}= 0.0016 p.u., i.e. 1.32 µF, is chosen. This value allows to leave enough capacitance left for possible trap filters damping circuits, with respect to the already used capacitance and the C_{max_PF} limit calculated at step 1. Consequently, the two inductances are chosen to be L_{TR_F1}= 0.01 p.u. (133 µH), and L_{TR_F2}= 0.0026 p.u., (33.3 µH), on the basis of obtainable inductance values with available cores. When sizing 24 kHz trap filter, instead of halving 12 kHz trap filter components' values, it is chosen to use the same capacitor value, reducing the trap inductance to about 25%. This action allows to slightly widening the 24 kHz trap filter transfer function shape at the resonance, with respect to the 12 kHz trap filter, thus providing a better ability to follow the sidebands profile close to the second harmonic switching component. Results of this design step are depicted in Fig.9. It is possible to note how, even if the trap filters present a limited frequency range of influence, their presence somewhat affects also the LC_{main} and DMP_{LC} related dynamics, as previously seen in Fig. 6.

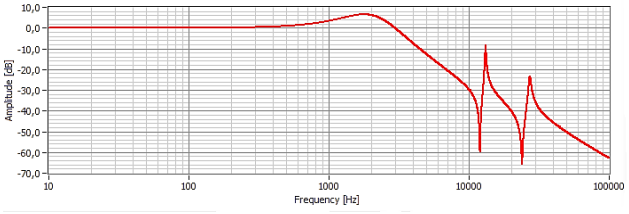

Figure 9. LC_{main} + DMP_{LC} + trap filters design results.

D. *Step 4, damping of the trap filters*

With reference to Fig. 2, the DMP_{F1} and DMP_{F2} tuning frequencies are selected to be, accordingly to given criteria, approximately 12.8 kHz and 27 kHz. The remaining capacitance with respect to C_{max_PF} value allows to choose a 0.0006 p.u., (0.47 µF), capacitor for each damping circuit. The corresponding needed inductances are respectively L_{DMP_F1}= 0.026 p.u., (330 µH), and L_{DMP_F2}= 0.0057 p.u., (73 µH). R_{DMP_F1}= 1.18 p.u., (4.7 Ω), and R_{DMP_F2}= 0.75 p.u., (3 Ω), as damping resistors are found to provide proper results based on selected components. Fig.10 shows the effect of adding DMP_{F1} and DMP_{F2} circuit to the filter so far designed.

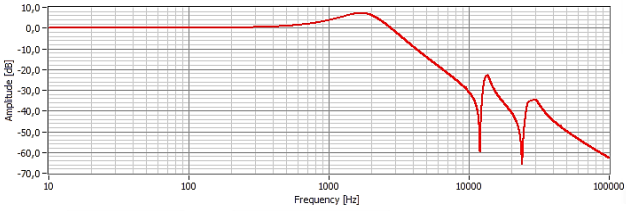

Figure 10. Complete filter design results.

V. Evaluation of the Proposed Filter Configuration

The proposed filter configuration is evaluated through its investigation in the frequency domain versus the more conventional LC and LCL filter topologies, shown respectively in Fig. 11a and 11b. Tab. I summarizes the parameters' values for the three filter configurations with reference to the schematics of Fig. 2 and Fig. 11; where the parameters' values are selected with the purpose to achieve similar behavior, for the three compared filter topologies, in the frequency domain. The proposed filter topology is investigated, in off-grid mode of operation, through the Bode diagram of Fig. 12 and compared with LCL and LC filters performance. The proposed arrangement uses only one power inductor, compared to the LCL configuration, and a smaller main capacitor, compared to the LC topology.

In the investigated filter, the resonance frequency can be maintained in the region of few kHz without sacrificing the filter roll-off at high frequencies. Same feature is hardly achieved with the LC filter, which for the described comparison has been sized considering a trade-off between high frequency attenuation and both resonance frequency (mainly related to capacitor size) and roll-off (strongly related to damping resistor size).

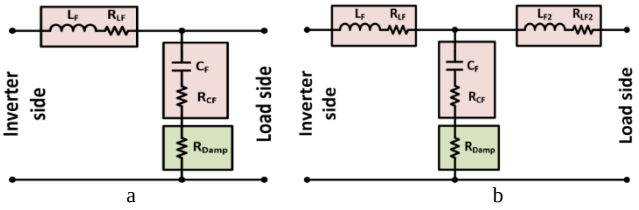

Figure 11. Filter topologies, a) LC, b) LCL.

TABLE I. FILTERS COMPONENTS' VALUES

	Proposed Filter		LCL		LC	
Component	*Value*	*p.u.*	*Value*	*p.u.*	*Value*	*p.u.*
L_F [µH]	750	0.0593	738	0.0584	750	0.0593
C_F [µF]	5	0.0062	6.5	0.0081	50	0.0623
L_{DMP_LC} [µH]	810	0.0641	–	–	–	–
C_{DMP_LC} [µF]	7.2	0.009	–	–	–	–
R_{DMP_LC} [Ω]	20	5.038	1.44	0.3627	4	1.0075
L_{F2} [µH]	–	–	147	0.0116	–	–
L_{TR_F1} [µH]	133	0.0105	–	–	–	–
C_{TR_F1} [µF]	1.32	0.0016	–	–	–	–
L_{TR_F2} [µH]	33.3	0.0026	–	–	–	–
C_{TR_F2} [µF]	1.32	0.0016	–	–	–	–
L_{DMP_F1} [µH]	330	0.0261	–	–	–	–
C_{DMP_F1} [µF]	0.47	0.0006	–	–	–	–
R_{DMP_F1} [Ω]	4.7	1.1839	–	–	–	–
L_{DMP_F2} [µH]	73	0.0058	–	–	–	–
C_{DMP_F2} [µF]	0.47	0.0006	–	–	–	–
R_{DMP_F2} [Ω]	3	0.7557	–	–	–	–

The LCL filter topology has been sized with reference to the procedure illustrated in [1]. According to it, the damping resistor value has been chosen quite small in order to not degrade filter roll-off. This, in turn, has led to a partially damped resonance that, especially in standalone operation mode, could produces malfunction to the entire system. The use of the RLC branch to damp the main LC filter section in the proposed filter topology allows to effectively diminishing the resonance of the filter, while assuring its second order -40 dB/dec roll-off.

In Fig. 12 the three filter topologies have been compared for different load conditions and in off-grid mode of operation. As previously mentioned, the no load condition is the most critical concerning the filter behavior at the resonance. When the filters are designed with reference to no-load mode of operation, as it is shown in Fig. 12a, performance at power factor even significantly lower than 1 are still acceptable, as depicted in Fig. 12b and c. For any of the investigated operating condition, the proposed arrangement has shown to achieve at least 30 dB more attenuation with respect to LCL and LC topologies, in the frequency range from 100 kHz to 1 MHz. As a result, the additional EMC filter stage can be reduced in both dimensions and weight. Moreover, the phase voltage ripple content of Fig. 13 is dramatically reduced in the proposed filter with respect to the other topologies, because of the use of the LC trap branches. However, power losses, cost and overall volume of the proposed filter must be evaluated as a result of the addition of further passive components in damping and trap branches.

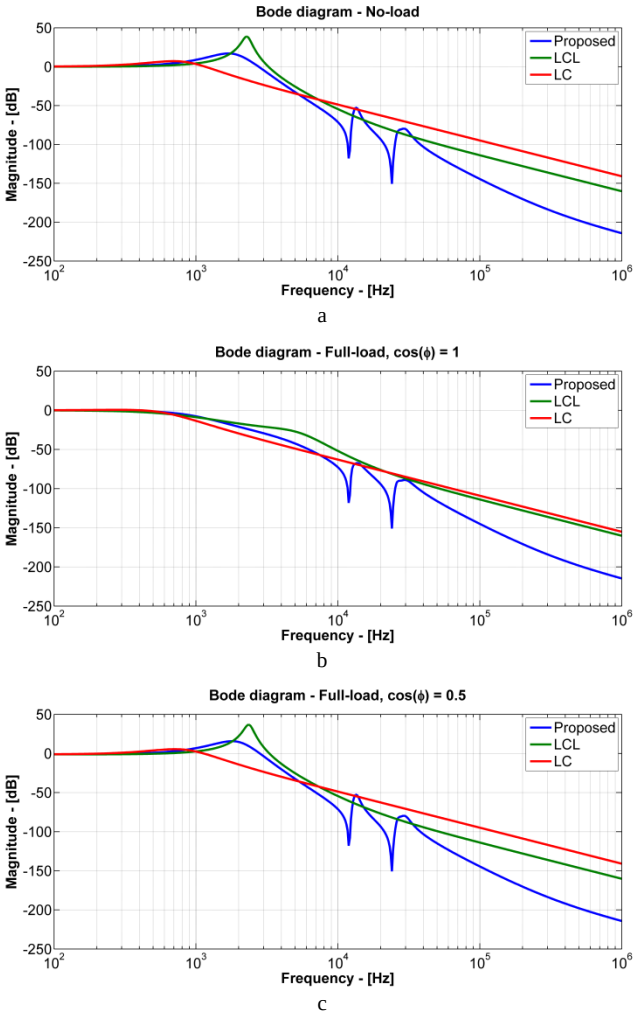

Figure 12. Bode diagrams at different operating conditions, a) no-load, b) full-load and cos(φ) = 1, c) full-load and cos(φ) = 0.5.

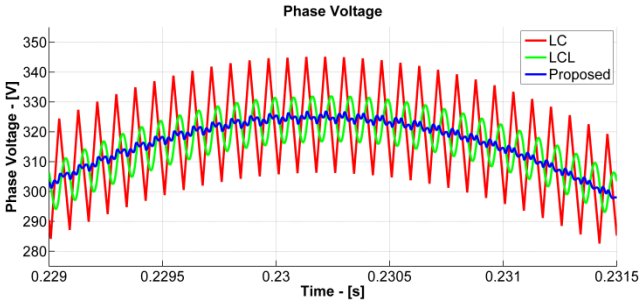

Figure 13. Phase voltage ripple content, LC topology (red trace), LCL topology (green trace), proposed filter (blue trace).

VI. POWER LOSSES ESTIMATION

Filter power losses are mainly located in the LC_{main} inductor and depend on core material and winding type. For this reason, an inductor with Metglas® core and Litz wire

winding is chosen. The combination of this two type of technologies allows to consistently reducing high frequency related power losses, by lowering core material losses and winding losses due to skin and proximity effects, with respect to standard laminated cores with solid copper windings.

For what concerns the other filter's elements, power losses estimation is calculated on the basis of the following assumptions. If the filter is properly designed, output voltage (i.e. voltage across trap filters, LC_{main} capacitor and DMP_{LC} circuits) contains only a small component at switching frequency and its multiplies. This allows to assume that the only current flowing into DMP_{LC} circuits is at the fundamental frequency, so it is possible to estimate the power losses on R_{DMP_LC} as

$$P_{R\_DMP\_LC} = R_{DMP\_LC} \cdot I^2_{DMP\_LC\_rms} \tag{4}$$

where

$$I_{DMP\_LC\_rms} \approx \frac{V_{OUT\_PH\_rms}}{\left| Z_{DMP\_LC}\left(f = f_{fund} \right) \right|} \tag{5}$$

Using (4) and (5), the previously selected components values and R_{DMP_LC}=20 Ω lead to the estimated dissipation of 5.41W.

Trap filters related power losses have been evaluated taking into consideration their selective behavior, as well assuming that only the respective switching components and related sidebands flow through them. Moreover, around the resonance frequency, the impedance of the trap filters is so small that for this analysis it is possible to neglect the presence of both LC_{main} capacitor, DMP_{LC} circuit and other trap filters tuned at different frequencies, thus reducing the circuit to only LC_{main} inductor and the trap impedance (i.e. trap ESR resistance). Under the above assumptions and taking in consideration the output voltage spectrum of (1), it is possible to evaluate the peak current in the trap filter as the sum of the currents related to the output voltage switching component and its sidebands

$$I_{TRAP\_pk} = \sum_n \frac{V_{OUT\_pk}\left(f_{sw} + n \cdot f_{fund} \right)}{\left| Z_{TRAP\_pk}\left(f_{sw} + n \cdot f_{fund} \right) \right|} \tag{6}$$

The value of *n* from -20 to 20 has been found to cover all the main frequency contributions. In this way, with selected components values, it is estimated a current value of about 8 A and 3.5 A respectively for TF_{F1} and TF_{F2}. As a result, from core material datasheet and neglecting power losses on ESR resistances, power losses have been estimated 1.48 W and 0.77 W for respectively TF_{F1} and TF_{F2} trap filters.

Power losses in trap dampers can be neglected without any lack of accuracy. This assumption is reasonable because the frequency region of interest for trap dampers contains only small amplitude sideband harmonics, which are already attenuated by trap filter circuits. The presence of trap damper circuits is, in fact, devoted to properly shape traps behavior around the resonance point, in order to avoid amplification of switching sidebands caused by the interaction of trap filters with LC_{main} filter.

Comparison of the theoretical power losses for the proposed filter vs. both LCL and LC configurations has also been accomplished. Basically, the same main inductor L_f is considered for the three filter topologies; as a result, difference in power losses is related to the main capacitor C_f, to the additional passive components and mainly to the required damping resistors. In order to accomplish the power losses comparison, the top characteristics of a number of devices (i.e. inductors, capacitors, and damping resistors) from the most important manufacturers (i.e. EPCOS, KEMET, VISHAY) have been selected. Results of the theoretical investigation are achieved at full load and off-grid mode of operation. Table II shows the clear superior performance of the proposed filter, exclusively related to the lower current RMS value in the main damping resistor. Values in p.u. of the filter total power losses are the direct indication of the decrease in efficiency due to the filter itself.

Cost comparison for the three filter topologies is achieved on the basis of devices cost, reported by the international main distributors of electric and electronic components. Table III summarizes calculated devices' costs, it also shows total cost per kVA for each filter. The cost of the additional components in the proposed filter is exceeded by the higher cost related to the required damping resistor and pertinent heat sink if any in LC topology, as well by the higher cost related to the output inductor L_{f2} in LCL configuration. Table III gives also information on total cost per kVA; whereas, the estimated total overall dimensions are very similar for the three considered filter solutions and approximately measure 28cm x 38cm x 18cm (LxWxH), which turns in 0.48 dm^3/kVA.

Neglecting the contribution of base plate and mechanical cover, the total weight per kVA of the proposed filter results in 0.425kg/kVA. The LCL configuration reaches 0.525kg/kVA because of the weight of the output inductor L_{f2}; whereas, the LC topology is affected by the damping resistors and pertinent cooling plate weight, which are sized according to the estimated power losses.

TABLE II. POWER LOSSES IN THE FILTER TOPOLOGIES

	Proposed Filter	**LCL**	**LC**
Power Losses	*Value [W]*	*Value [W]*	*Value [W]*
L_F winding	37	37	37
L_F core	11	11	11
C_F ESR	0.006	0.193	0.076
R_{DMP_LC}	5	39.69	134.56
L_{F2} winding	–	7.35	–
L_{F2} core	–	2.2	–
Traps sections	2.29	–	–
Traps' dampers	1.25	–	–
Total 1 phase	56.55	97.43	182.64
Total 3 phase	169.65	292.29	547.92
Total [p.u.]	0.0042	0.0073	0.0137

TABLE III. AVERAGE COST OF FILTER TOPOLOGIES

	Proposed Filter	**LCL**	**LC**
Component	*Cost [€]*	*Cost [€]*	*Cost [€]*
L_F	65	65	65
C_F	3.4	3.4	25
Damper	10	5.5	30
L_{F2}	–	30	–
$Trap_1$	5	–	–
$Trap_1$ Damper	4.1	–	–
$Trap_2$	4	–	–
$Trap_2$ Damper	4.1	–	–
Total 1 phase	95.6	103.9	120
Total 3 phase	286.8	311.7	360
Cost per power unit [€/kVA]	7.17	7.79	9

VII. EXPERIMENTAL RESULTS

A prototype of the proposed filter has been arranged as shown in Fig. 14 and tested. Selected components' values are listed in Table I. The filter prototype dimensions are about 32 cm x 38 cm x 18 cm (L x W x H) also including the EMC stage. This means the power density of about 2 kVA per dm^3, that can be easily increased optimizing filter layout power connections.

Consistency of filter's calculated transfer function with prototype transfer function has been checked measuring filter's frequency response with the HP4192A Impedance Analyzer. Results of this comparison are illustrated in Fig. 15 and show a good accordance between the designed and the actual prototype transfer functions. The only appreciable differences are in the region of LC_{main} resonance frequency and at high frequencies. The first difference is due to components' tolerances of both LC_{main} inductors and wire-wound metal clad resistors used for R_{DMP_LC}; whereas, the second difference is the effect of the interaction of the proposed filter architecture with the EMC filter stage, added to comply with international standards. In order to investigate the prototype performances for both on-grid and off-grid modes of operation, a 4-leg 4-wire inverter, able to switch between the two modes, has been used.

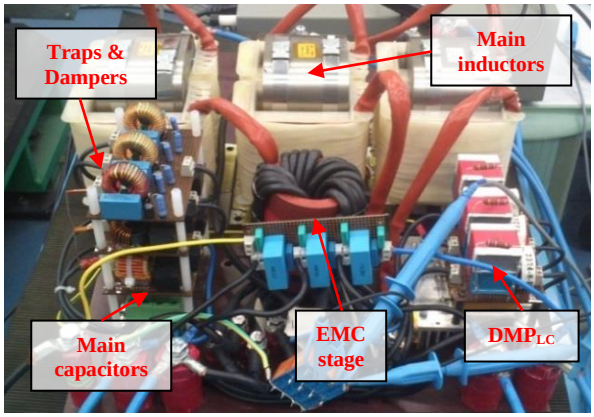

Figure 14. Prototype of the proposed filter.

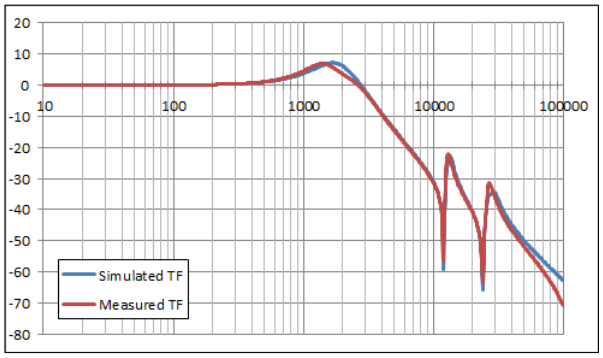

Figure 15. Simulated and measured filter transfer functions comparison.

The filter has been equipped, as previously mentioned, with additional common mode inductor, X and Y capacitors, in order to comply with current international EMC standards. The inverter was operated supplying a 12 kW three-phase resistive load for both on-grid and off-grid configuration. Implemented inverter control structure has been investigated in [15] at numerous different load conditions when the inverter is operated in islanding mode. Whereas, during grid-tied operation, control tuning and stabilization are accomplished according to [16, 17].

The proposed control strategy is based on Integral and Resonant combined topologies, which is a well-know control architecture working directly on the stationary reference frame. The complete control algorithm makes use of three voltage sensors and three current sensors at the inverter side and they are used in both grid-tied and stand-alone modes of operation. Three additional voltage sensors are located at the grid-side and they are used for grid synchronization and grid parameters assessment. The switch between on-grid and off-grid configurations is achieved though an external power breaker, whereas an algorithm for islanding detection is used to run the transition current-mode/voltage-mode. With reference to Fig. 16, in order to have a smooth transition in current waveforms, voltage/current mode control is based on the same Integral+Resonant structure, where controller references and measures are switched according to the operating condition. Reference voltage signals (V_{ref}) are internally generated by the control unit and they are locked to the grid voltages until the power breaker opens, i.e. islanding condition is detected. Then, the used control reference and measure signals are moved from current (I_{ref} and I_{ph}) to voltage (V_{ref} and V_{ph}), avoiding discontinuities. The *Switch* block shown in Fig. 16 acts to correctly modify the voltage references when the islanding detection condition in detected. During grid-tied operation the internally generated voltage references are continuously synchronized with the grid voltages. At off-grid transition, the inverter output voltages continue at first to follow the grid-synched voltages just before islanding mode, and then they evolve following the internally generated frequency source, thus avoiding any discontinuity. Achieved results are shown in Fig. 17 and Fig.18.

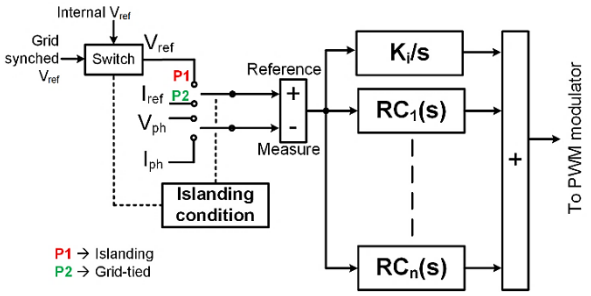

Figure 16. Block scheme of the control algorithm for both grid-tied and stand-alone modes of operation.

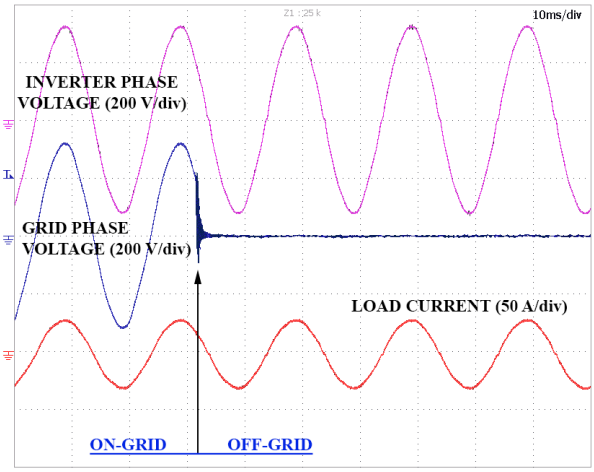

Figure 17. On-grid to Off-grid mode of operation with 12 kW three-phase resistive load.

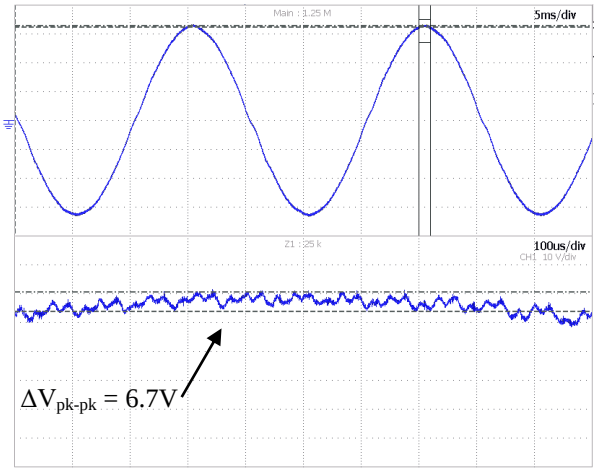

Figure 18. Line to neutral voltage at no-load.

Transition from on-grid to off-grid configuration is depicted in Fig. 17, it shows that both current and voltage waveforms at the supplied load are not affected during the change in the operation mode. In Fig. 18, output phase voltage waveform, at no-load and in off-grid mode, has been zoomed in order to measure residual peak-to-peak switching ripple. The off-grid mode is in fact the worst-case mode of operation for what concerns output voltage quality; further, the no-load condition is critical for the output voltage waveform because the voltage is not imposed by the grid and the filter behavior can be influenced by connected loads. Measured residual peak-to-peak switching voltage is about 6.7 V_{pk-pk}, which corresponds to 3.35 V of voltage ripple, very similar to the expected value of 3.25 V, calculated as 1% of the peak voltage of the 230Vrms rated phase voltage.

Power losses analysis has been performed in off-grid mode and at both no-load and rated power conditions. The no-load analysis allows to measure core's material, skin and proximity effect related power losses in the LC_{main} inductor, whereas the full-load analysis allows to measure the Joule effect related power losses. Power measures have been performed by means of the Voltech PM3000 power analyzer, current and voltage probes were positioned directly on filter's elements or circuits of interest. Results referred to a single phase of the 3-phase filter are depicted in Table IV. The entire filter prototype power losses have been found to be about 55 W at no-load and 170 W at full-load, i.e. respectively less than 0.14% and 0.42% of the converter rated power of 40 kVA.

TABLE IV. FILTER PROTOTYPE POWER MEASURES PER PHASE

Component	Power [W]
Inductor LC_{main} (no-load)	10.2
Inductor LC_{main} (full-load)	48.3
Capacitor LC_{main}	~0
DMP_{LC} circuit	5.8
TF_{F1} circuit	1.5
TF_{F2} circuit	0.8
DMP_{F1} circuit	~0
DMP_{F2} circuit	~0
Total (no-load)	18.3
Total (full-load)	56.4

VIII. CONCLUSIONS

In this paper, the complete filter design procedure for distributed generating units, able to operate in both on-grid and off-grid modes, is illustrated. Main criteria for sizing each filter section are given and explained. An example design procedure has been performed, in order to demonstrate the accuracy of the proposed criteria. The comparison with the more conventional LCL and LC filter topologies proves a substantial superiority of the performance of the proposed filter configuration. On-grid and off-grid modes of operation have been also experimentally tested in order to verify filter performances with respect to current and voltage waveforms. Power losses measurements on the proposed prototype have been carried out too, and they show good agreement with estimated values.

APPENDIX A

For the LC_{main} circuit with the cascaded trap filter TF_{F1} in parallel with LC capacitor, the transfer function of Fig. 6, neglecting R_{Lesr} and R_{Cesr}, can be written as

$$G(s)=\frac{k_2^2\left(s^2+k_1 s+k_3^2\right)}{s^4+k_1 s^3+\left(k_2^2+k_4^2+k_3^2\right)s^2+\left(k_1 k_2^2\right)s+\left(k_2^2 k_3^2\right)} \quad \text{(A1)}$$

where

$$k_1 = R_{TR\_F1}/L_{TR\_F1}$$
$$k_2 = 1/\sqrt{C_F L_F}$$
$$k_3 = 1/\sqrt{C_{TR\_F1} L_{TR\_F1}}$$
$$k_4 = 1/\sqrt{C_F L_{TR\_F1}}$$

In (A1), filter's parameters have been grouped in k_1, k_2, k_3, and k_4 terms in order to shrink the complete expression.
If R_{TR_F1}=0, (A1) becomes

$$G(s)=\frac{k_2^2\left(s^2+k_3^2\right)}{s^4+\left(k_2^2+k_4^2+k_3^2\right)s^2+\left(k_2^2 k_3^2\right)} \quad \text{(A2)}$$

Equation (A2) can be re-written making use of two second grade polynomials as

$$G(s)=\frac{k_3^2\left(s^2+\omega_T^2\right)}{\left(s^2+\omega_1^2\right)\left(s^2+\omega_2^2\right)} \quad \text{(A3)}$$

with

$$\omega_T = k_3 = 1/\sqrt{C_{TR\_F1} L_{TR\_F1}}$$
$$\omega_{1,2}=\sqrt{\frac{\left(k_2^2+k_4^2+k_3^2\right)\pm\sqrt{\left(k_2^2+k_4^2+k_3^2\right)^2-4\left(k_2^2 k_3^2\right)}}{2}} \quad \text{(A4)}$$

where ω_T, ω_1 and ω_2 are, respectively, the frequency of the notch and the frequencies of the two resonance peaks of the transfer function shown in Fig. 6.

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